FET PRINCIPLES AND CIRCUITS

Part 1

Field-Effect Transistors

by Ray Marston

Ray Marston explains FET (Field-Effect Transistor) basics in this opening episode of this new four-part series.

Field-Effect Transistors (FETs) are unipolar devices, and have two big advantages over bipolar transistors: one is that they have a near-infinite input resistance and thus offer near-infinite current and power gain; the other is that their switching action is not marred by charge-storage problems, and they thus outperform most bipolars in terms of digital switching speeds.

Several different basic types of FETs are available, and this opening episode looks at their basic operating principles. Parts 2 to 4 of the series will show practical ways of using FETs.

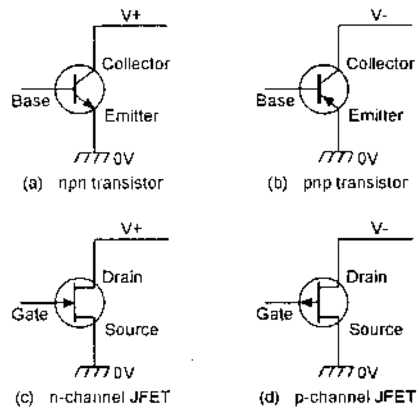


***Figure 1.* Comparison of transistor and JFET symbols, notations, and supply polarities.**

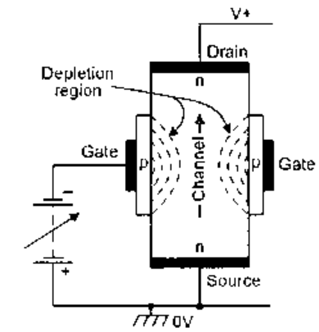


***Figure 2.* Basic structure of a simple n-channel JFET, showing how channel width is controlled via the gate bias.**

FET BASICS

An FET is a three-terminal amplifying device. Its terminals are known as the source, gate, and drain, and correspond respectively to the emitter, base, and collector of a normal transistor. Two distinct families of FETs are in general use. The first of these is known as 'junction-gate' types of FETs; this term generally being abbreviated to either JUGFET or (more usually) JFET.

The second family is known as either 'insulated-gate' FETs or Metal Oxide Semiconductor FETs, and these terms are generally abbreviated to IGFET or MOSFET, respectively. 'N-channel' and 'p-channel' versions of both types of FET are available, just as normal transistors are available in npn and pnp versions. *Figure 1* shows the symbols and supply polarities of both types of bipolar transistor, and compares them with both JFET versions.

Figure 2 illustrates the basic construction and operating principles of a simple n-channel JFET. It consists of a bar of n-type semiconductor material with a drain terminal at one end and a source terminal at the other. A p-type control electrode or gate surrounds (and is joined to the surface of) the middle section of the n-type bar, thus forming a p-n junction.

In normal use, the drain terminal is connected to a positive supply and the gate is biased at a value that is negative (or equal) to the source voltage, thus reverse-biasing the JFET's internal p-n junction, and accounting for its very high input impedance.

With zero gate bias applied, a current flow from drain to source via a conductive 'channel' in the n-type bar is formed. When negative gate bias is applied, a high resistance region is formed within the junction, and reduces the width of the n-type conduction channel and thus reduces the magnitude of the drain-to-source current. As the gate bias is increased, the 'depletion' region spreads deeper into the n-type channel, until eventually, at some 'pinch-off' voltage value, the depletion layer becomes so deep that conduction ceases.

Thus, the basic JFET of *Figure 2* passes maximum current when its gate bias is zero, and its current is reduced or 'depleted' when the gate bias is increased. It is thus known as a 'depletion-type' n-channel JFET. A p-channel version of the device can (in principle) be made by simply transposing the p and n materials.

JFET DETAILS

Figure 3 shows the basic form of construction of a practical n-channel JFET; a p-channel JFET can be made by transposing the p and n materials. All JFETs operate in the depletion mode, as already described. *Figure 4* shows the typical transfer characteristics of a low-power n-channel JFET, and illustrates some important features of this type of device. The most important characteristics of the JFET are as follows:

(1). When a JFET is connected to a supply with the polarity shown in *Figure 1* (drain +ve for an n-channel FET, -ve for a p-channel FET), a drain current (I_D) flows and can be controlled via a gate-to-source bias voltage V_{GS}.

(2). I_D is greatest when V_{GS} = 0, and is reduced by applying a reverse bias to the gate (negative bias in an n-channel device, positive bias in a p-type). The magnitude of V_{GS} needed to reduce I_D to zero is called the 'pinch-off' voltage, V_P, and typically has a value between 2 and 10 volts. The magnitude of I_D when V_{GS} = 0 is denoted I_{DSS}, and typically has a value in the range 2 to 20mA.

(3). The JFET's gate-to-source junction has the characteristics of a silicon diode. When reverse-biased, gate leakage currents (I_{GSS}) are only a couple of nA (1nA = .001μA) at room temperature. Actual gate signal currents are only a fraction of an nA, and the input impedance of the gate is typically thousands of megohms at low frequencies. The gate junction is shunted by a few pF, so the input impedance falls as frequency rises.

If the JFET's gate-to-source junction is forward-biased, it conducts like a normal silicon diode. If it is excessively reverse-biased, it

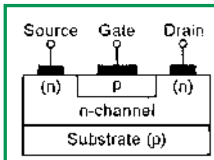


***Figure 3.* Construction of n-channel JFET.**

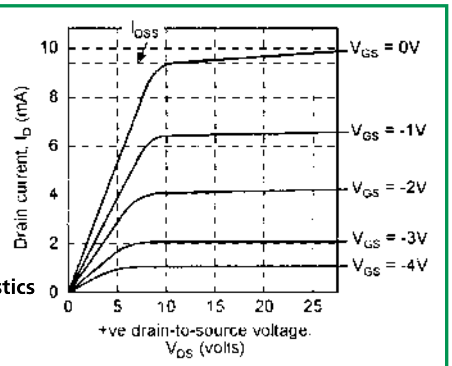


***Figure 4.* Idealized transfer characteristics of an n-channel JFET.**

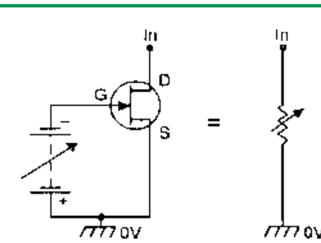


***Figure 5.* An n-channel JFET can be used as a voltage-controlled resistor.**

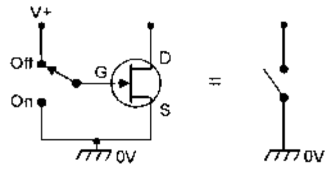


***Figure 6.* An n-channel JFET can be used as a voltage-controlled switch.**

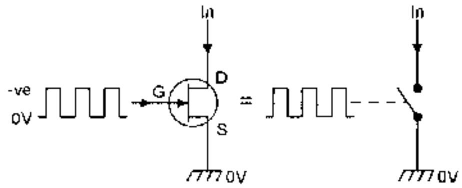
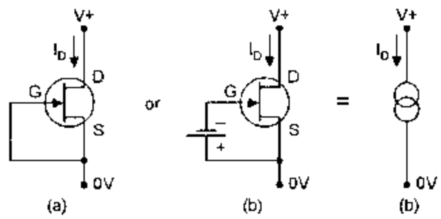


***Figure 7.* An n-channel JFET can be used as an electronic chopper.**

***Figure 8.* An n-channel JFET can be used as a constant-current generator.**



avalanches like a zener diode. In either case, the JFET suffers no damage if gate currents are limited to a few mA.

(4). Note in *Figure 4* that, for each V_{GS} value, drain current I_D rises linearly from zero as the drain-to-source voltage (V_{DS}) is increased from zero up to some value at which a 'knee' occurs on each curve, and that I_D then remains virtually constant as V_{DS} is increased beyond the knee value. Thus, when V_{DS} is below the JFET's knee value, the drain-to-source terminals act as a resistor, R_{DS}, with a value dictated by V_{GS}, and can thus be used as a voltage-variable resistor, as in *Figure 5*.

Typically, R_{DS} can be varied from a few hundred ohms (at V_{GS} = 0) to thousands of megohms (at $V_{GS} = V_P$), enabling the JFET to be used as a voltage-controlled switch (*Figure 6*) or as an efficient 'chopper' (*Figure 7*) that does not suffer from offset-voltage or saturation-voltage problems.

Also note in *Figure 4* that when V_{DS} is above the knee value, the I_D value is controlled by the V_{GS} value and is almost independent of V_{DS}, i.e., the JFET acts as a voltage-controlled current generator. The JFET can be used as a fixed-value current generator by either tying the gate to the source as in *Figure 8(a)*, or by applying a fixed negative bias to the gate as in *Figure 8(b)*. Alternatively, it can (when suitably biased) be used as a voltage-to-current signal amplifier.

(5). FET 'gain' is specified as transconductance, g_m, and denotes the magnitude of change of drain current with gate voltage, i.e., a g_m of 5mA/V signifies that a V_{GS} variation of one volt produces a 5mA change in I_D. Note that the form I/V is the inverse of the ohms formula, so g_m measurements are often expressed in 'mho' units. Usually, g_m is specified in FET data sheets in terms of mmhos (milli-mhos) or µmhos (micro-mhos). Thus, a g_m of 5mA/V = 5-mmho or 5000-µmho.

In most practical applications, the JFET is biased into the linear region and used as a voltage amplifier. Looking at the n-channel JFET, it can be used as a common source amplifier (corresponding to the bipolar npn common emitter amplifier) by using the basic connections in *Figure 9*.

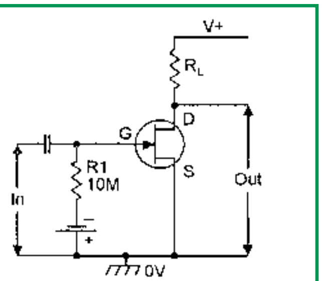


***Figure 9.* Basic n-channel common-source amplifier JFET circuit.**

Alternatively, the common drain or source follower (similar to the bipolar emitter follower) configuration can be obtained by using the connections in *Figure 10*, or the common gate (similar to common base) configuration can be obtained by using the basic *Figure 11* circuit. In practice, fairly accurate biasing techniques (discussed in Part 2 of this series) must be used in these circuits.

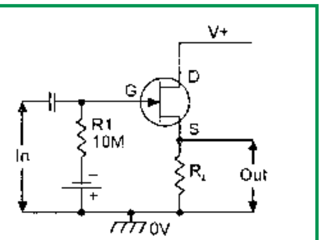


***Figure 10.* Basic n-channel common-drain (source-follower) JFET circuit.**

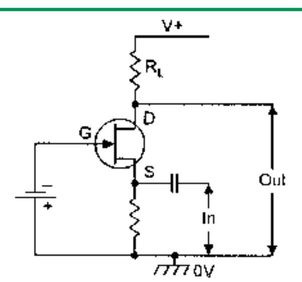


***Figure 11.* Basic n-channel common-gate JFET circuit.**

THE IGFET/MOSFET

The second (and most important) family of FETs are those known under the general title of IGFET or MOSFET. In these FETs, the gate terminal is insulated from the semiconductor body by a very thin layer of silicon dioxide, hence the title 'Insulated Gate Field Effect Transistor,' or IGFET. Also, the devices generally use a 'Metal-Oxide Silicon' semiconductor material in their construction, hence the alternative title of MOSFET.

Figure 12 shows the basic construction and the standard symbol of the n-channel depletion-mode FET. It resembles the JFET, except that its gate is fully insulated from the body of the FET (as indicated by the *Figure 12(b)* symbol) but, in fact, operates on a slightly different principle to the JFET.

It has a normally-open n-type channel between drain and source, but the channel width is controlled by the electrostatic field of the gate bias. The channel can be closed by applying suitable negative bias, or can be increased by applying positive bias.

In practice, the FET substrate may be externally available, making a four-terminal device, or may be internally connected to the source, making a three-terminal device.

An important point about the IGFET/MOSFET is that it is also available as an enhancement-mode device, in which its conduction channel is normally closed but can be opened by applying forward bias to its gate.

Figure 13 shows the basic construction and the symbol of the n-channel version of such a device. Here, no n-channel drain-to-source conduction path exists through the p-type substrate, so with zero gate bias there is no conduction between drain and source; this feature is indicated in the symbol of *Figure 13(b)* by the gaps between source and drain.

To turn the device on, significant positive gate bias is needed, and when this is of sufficient magnitude, it starts to convert the p-type substrate material under the gate into an n-channel, enabling conduction to take place.

Figure 14 shows the typical transfer characteristics of an n-channel enhancement-mode IGFET/MOSFET, and *Figure 15* shows the V_{GS}/I_D curves of the same device when powered from a 15V supply. Note that no I_D current flows until the gate voltage reaches a 'threshold' (V_{TH}) value of a few volts, but that beyond this value, the drain current rises in a non-linear fashion.

Also note that the transfer graph is divided into two characteristic regions, as indicated (in *Figure 14*) by the dotted line, these being the 'triode' region and the 'saturated' region. In the triode region, the device acts like a voltage-controlled

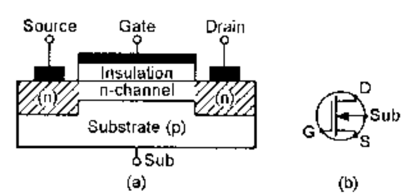


***Figure 12.* Construction (a) and symbol (b) of n-channel depletion-mode IGFET/MOSFET.**

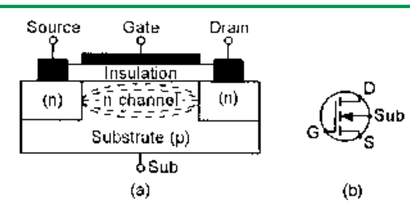


***Figure 13.* Construction (a) and symbol (b) of n-channel enhancement-mode IGFET/MOSFET.**

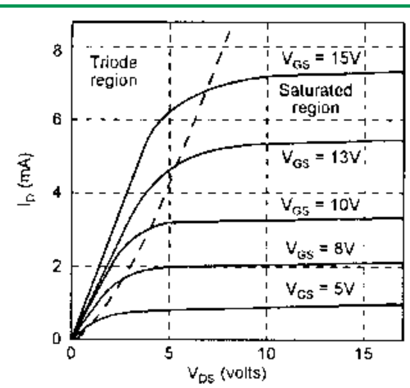


***Figure 14.* Typical transfer characteristics of n-channel enhancement-mode IGFET/MOSFET.**

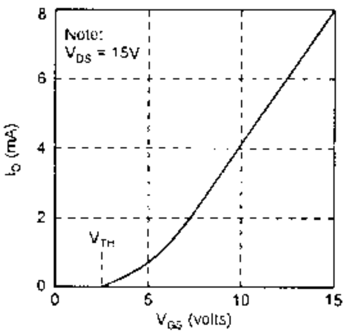


***Figure 15.* Typical V_{GS}/I_D characteristics of n-channel enhancement-mode IGFET/MOSFET**

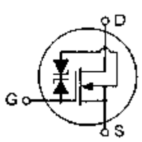


***Figure 16.* Internally-protected n-channel depletion-mode IGFET/MOSFET.**

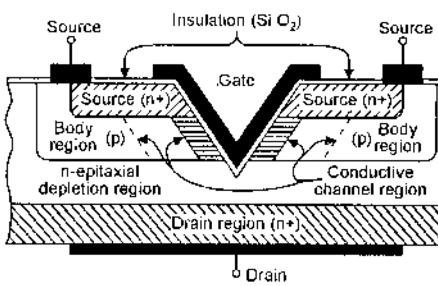


***Figure 17.* Basic structure of the VFET power device.**

resistor; in the saturated region, it acts like a voltage-controlled constant-current generator.

The basic n-channel MOSFETs of *Figures 12* and *13* can — in principle — be converted to p-channel devices by simply transposing their p and n materials, in which case their symbols must be changed by reversing the directions of their substrate arrows.

A number of sub-variants of the MOSFET are in common use. The type known as 'DMOS' uses a double-diffused manufacturing technique to provide it with a very short conduction channel and a consequent ability to operate at very high switching speeds. Several other MOSFET variants are described in the remainder of this opening episode.

Note that the very high gate impedance of MOSFET devices makes them liable to damage from electrostatic discharges and, for this reason, they are often provided with internal protection via integral diodes or zeners, as shown in the example in *Figure 16*.

VFET DEVICES

In a normal small-signal JFET or MOSFET, the main signal current flows 'laterally' (see *Figures 3, 12*, and *13*) through the device's conductive channel. This channel is very thin, and maximum operating currents are consequently very limited (typically to maximum values in the range 2 to 40mA).

In post-1970 times, many manufacturers have tried to produce viable high-power/high-current versions of the FET, and the most successful of these have relied on the use of a 'vertical' (rather than lateral) flow of current through the conductive channel of the device. One of the best known of these devices is the 'VFET,' an enhancement-mode power MOSFET which was first introduced by Siliconix way back in 1976.

Figure 17 shows the basic structure of the original Siliconix VFET. It has an essentially four-layer structure, with an n-type source layer at the top, followed by a p-type 'body' layer, an epitaxial n-type layer, and (at the bottom) an n-type drain layer. Note that a 'V' groove (hence the 'VFET' title) passes through the first two layers and into the third layer of the device, and is electrostatically connected (via an insulating silicon dioxide film) to the gate terminal.

If the gate is shorted to the source, and the drain is made positive, no drain-to-source current flows, because the diode formed by the p and n materials is reverse-biased. But if the gate is made positive to the source, the resulting electrostatic field converts the area of p-type material adjacent to the gate into n-type material, thus creating a conduction channel in the position shown in *Figure 17* and enabling current to flow vertically from the drain to the source.

As the gate becomes more positive, the channel width increases, enabling the drain-to-source current to increase as the drain-to-source resistance decreases. This basic VFET can thus pass reasonably high currents (typically up to 2A) without creating excessive current density within the channel regions.

The original Siliconix VFET design of *Figure 17* was successful, but imperfect. The sharp bottom of its V-groove caused an excessive electric field at this point and restricted the device's operating voltage. Subsequent to the original VFET introduction, Intersil introduced their own version of the 'VMOS' technique, with a U-shaped groove (plus other modifications) that improved device reliability and gave higher maximum operating currents and voltages. In 1980, Siliconix added these and other modifications to their own VFET devices, resulting in further improvements in performance.

OTHER POWER FETs

Several manufacturers have produced viable power FETs without using 'V'- or 'U'-groove techniques, but still relying on the vertical flow of current between drain and source. In the 1980s, Hitachi produced both p-channel and n-channel power MOSFET devices with ratings up to 8A and 200V; these devices were intended for use mainly in audio and low-RF applications.

Supertex of California and Farranti of England pioneered the development of a range of power MOSFETS with the general title of 'vertical DMOS.' These featured high operating voltages (up to 650V), high current rating (up to 16A), low on resistance (down to 50 milliohms), and very fast operating speeds (up to 2GHz at 1A, 500MHz at 10A).

Siemens of West Germany used a modified version of DMOS, known as SIPMOS, to produce a range of n-channel devices with voltage ratings as high as 1kV and with current ratings as high as 30A.

One International Rectifier solution to the power MOSFET problem is a device which, in effect, houses a vast array of parallel-connected low-power vertical MOSFETs or 'cells' which share the total current equally between them, and thus act like a single high-power MOSFET, as indicated in *Figure 18*. These devices are named HEXFET, after the hexagonal structure of these cells, which have a density of about 100,000 per square centimeter of semiconductor material.

Several manufacturers produce power MOSFETs that each comprise a large array of parallel-connected low-power lateral (rather than horizontal) MOSFET cells that share the total operating current equally between them; the device thus acts like a single high-power MOSFET. These high-power devices are known as *lateral* MOSFETs or L-MOSFETs, and give a performance that is particularly useful in super-fi audio power amplifier applications.

Note that, in parallel-connected MOSFETs (as used in the internal structure of the HEXFET and L-MOSFET devices described above), equal current sharing is ensured by the conduction channel's positive temperature coefficient; if the current in one MOSFET becomes excessive, the resultant heating of its channel raises its resistance, thus reducing its current flow and tending to equalize it with that of other parallel-connected MOSFETs. This feature makes such power MOSFETs almost immune to thermal runaway problems.

Today, a vast range of power MOSFET types are manufactured. 'Low voltage' n-channel types are readily available with voltage/current ratings as high as 100V/75A, and 'high voltage' ones with ratings as high as 500V/25A.

One of the most important recent developments in the power-MOSFET field has been the introduction of a variety of so-called 'intelligent' or 'smart' MOSFETs with built-in overload protection circuitry; these MOSFETs usually carry a distinctive registered trade name. Philips devices of this type are known as TOPFETs (Temperature and Overload Protected MOSFETs); *Figure 19* shows (in simplified form) the basic internal circuitry and the circuit symbol of the TOPFET.

The Siemens version of the smart MOSFET is known as the PROFET. PROFET devices incorporate protection against damage from short circuits, over temperature, overload, and electrostatic discharge (ESD). International Rectifier produce a

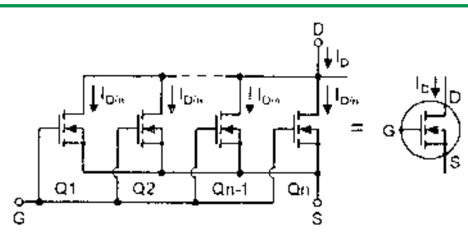


***Figure 18.* The IR HEXFET comprises a balanced matrix of parallel-connected low-power MOSFETs, which are equivalent to a single high-power MOSFET.**

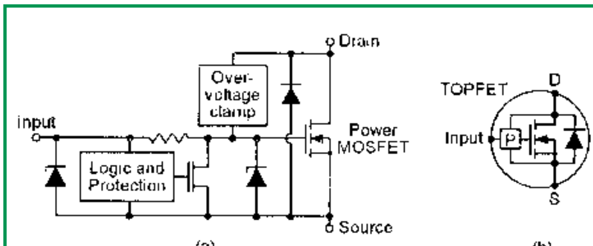


***Figure 19.* The basic internal circuitry (a) and the circuit symbol (b) of the TOPFET (Temperature and Overload Protected MOSFET).**

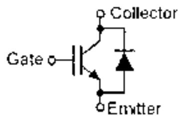


***Figure 20*. Normal circuit symbol of the IGBT (Insulated Gate Bipolar Transistor).**

range of smart n-channel MOSFET known as SMARTFETs; these incorporate protection against damage from short circuits, over temperature, overvoltage, and ESD.

Finally, yet another recent and important development in the n-channel power MOSFET field, has been the production — by various manufacturers — of a range of high power devices known as IGBTs (Insulated Gate Bipolar Transistors), which have a MOSFET-type input and an internally protected high-voltage high-current bipolar transistor output. *Figure 20* shows the normal circuit symbol of the IGBT. Devices of this type usually have voltage/current/power ratings ranging from as low as 600V/6A/33W (in the device known as the HGTD3N603), to as high as 1200V/520A/3000W (in the device known as the MG400Q1US51).

CMOS BASICS

One major FET application is in digital ICs. The best known range of such devices use the technology known as CMOS, and rely on the use of complementary pairs of *MOS*FETs. *Figure 21* illustrates basic CMOS principles. The basic CMOS device comprises a p-type and n-type pair of enhancement-mode MOSFETs, wired in series, with their gates shorted together at the input and their drains tied together at the output, as shown in *Figure 21(a)*. The pair are meant to use logic-0 or logic-1 digital input signals, and *Figures 21(b)* and *21(c),* respectively, show the device's equivalent circuit under these conditions.

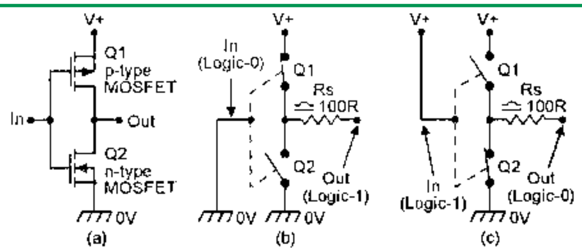


***Figure 21*. Basic CMOS circuit (a), and its equivalent with (b) a logic-0 input and (c) a logic-1 input.**

When the input is at logic-0, the upper (p-type) MOSFET is biased fully on and acts like a closed switch, and the lower (n-type) MOSFET is biased off and acts like an open switch; the output is thus effectively connected to the positive supply line (logic-1) via a series resistance of about 100R.

When the input is at logic-1, the MOSFET states are reversed, with Q1 acting like an open switch and Q2 acting like a closed switch, so the output is effectively connected to ground (logic-0) via 100R. Note in both cases that the entire signal current is fed to the load, and none is shunted off by the CMOS circuitry; this is a major feature of CMOS technology. **NV**

FET PRINCIPLES AND CIRCUITS

Part 2

Field-Effect Transistors

by Ray Marston

Ray Marston looks at practical JFET circuits in this second episode of this four-part series.

Last month's opening episode explained (among other things) the basic operating principles of JFETs. JFETs are low-power devices with a very high input resistance and invariably operate in the depletion mode, i.e., they pass maximum current when the gate bias is zero, and the current is reduced ('depleted') by reverse-biasing the gate terminal.

Most JFETs are n-channel (rather than p-channel) devices. Two of the oldest and best known n-channel JFETs are the 2N3819 and the MPF102, which are usually housed in TO92 plastic packages with the connections shown in *Figure 1*; *Figure 2* lists the basic characteristics of these two devices.

This month's article looks at basic usage information and applications of JFETs. All practical circuits shown here are specifically designed around the 2N3819, but will operate equally well when using the MPF102.

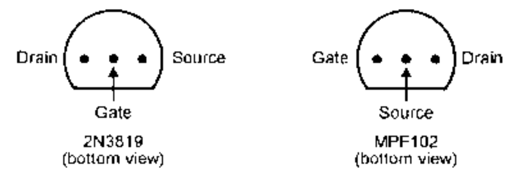


***Figure 1.* Outline and connections of the 2N3819 and MPF102 JFETs.**

Parameter	2N3918	MPF102
V_{DS} max (= max. drain-to-source voltage)	25V	25V
V_{DG} max (= max. drain-to-gate voltage)	25V	25V
V_{GS} max (= max. gate-to-source voltage)	-25V	-25V
I_{DSS} (= drain-to-source current with V_{GS} = 0V)	2-20mA	2-20mA
I_{GSS} max (= gate leakage current at 25° C)	2nA	2nA
P_T max (= max. power dissipation, in free air)	200mW	310mW

***Figure 2.* Basic characteristics of the 2N3819 and MPF102 n-channel JFETs.**

JFET BIASING

The JFET can be used as a linear amplifier by reverse-biasing its gate relative to its source terminal, thus driving it into the linear region. Three basic JFET biasing techniques are in common use. The simplest of these is the 'self-biasing' system shown in *Figure 3*, in which the gate is grounded via Rg, and any current flowing in Rs drives the source positive relative to the gate, thus generating reverse bias.

Suppose that an I_D of 1mA is wanted, and that a V_{GS} bias of -2V2 is needed to set this condition; the correct bias can obviously be obtained by giving Rs a value of 2k2; if I_D tends to fall for some reason, V_{GS} naturally falls as well, and thus makes I_D increase and counter the original change; the bias is thus self-regulating via negative feedback.

In practice, the V_{GS} value needed to set a given I_D varies widely between individual JFETS, and the only sure way of getting a precise I_D value in this system is to make Rs a variable resistor; the system is, however, accurate enough for many applications, and is the most widely used of the three biasing methods.

A more accurate way of biasing the JFET is via the 'offset' system of *Figure 4(a)*, in which divider R1-R2 applies a fixed positive bias to the gate via Rg, and the source voltage equals this voltage minus V_{GS}. If the gate voltage is large relative to V_{GS}, I_D is set mainly by Rs and is not greatly influenced by V_{GS} variations. This system thus enables I_D values to be set with good accuracy and without need for individual component selection. Similar results can be obtained by grounding the gate and taking the bottom of Rs to a large negative voltage, as in *Figure 4(b)*.

The third type of biasing system is shown in *Figure 5*, in which constant-current generator Q2 sets the I_D, irrespective of the JFET characteristics. This system gives excellent biasing stability, but at the expense of increased circuit complexity and cost.

In the three biasing systems described, Rg can have any value up to 10M, the top limit being imposed by the volt drop across Rg caused by gate leakage currents, which may upset the gate bias.

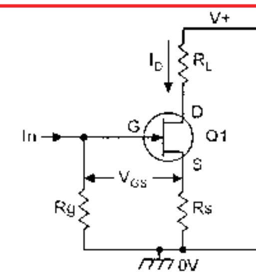


***Figure 3.* Basic JFET 'self-biasing' system.**

SOURCE FOLLOWER CIRCUITS

When used as linear amplifiers, JFETs are usually used in either the source follower (common drain) or common-source modes. The source follower gives a very high input impedance and near-unity voltage gain (hence the alternative title of 'voltage follower').

Figure 6 shows a simple self-biasing (via RV1) source follower; RV1 is used to set a quiescent R2 volt-drop of 5V6. The circuit's actual input-to-output voltage gain is 0.95. A degree of bootstrapping is applied to R3 and increases its effective impedance; the circuit's actual input impedance is 10M shunted by 10pF, i.e., it is 10M at very low frequencies, falling to 1M0 at about 16kHz and 100k at 160kHz, etc.

Figure 7 shows a source follower with offset gate biasing. Overall voltage gain is about 0.95. C2 is a bootstrapping capacitor and raises the input impedance to 44M, shunted by 10pF.

Figure 8 shows a hybrid (JFET plus bipolar) source follower. Offset biasing is applied via R1-R2, and constant-current generator Q2 acts as a very high-impedance source load, giving the circuit an overall voltage gain of 0.99. C2 bootstraps R3's effective impedance up to

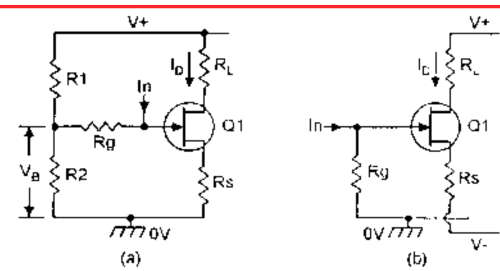


***Figure 4.* Basic JFET 'offset-biasing' system.**

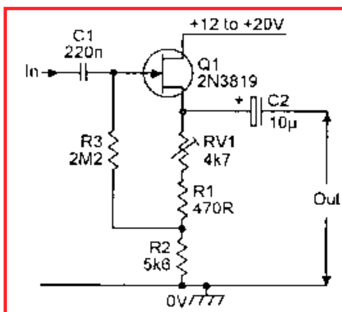


***Figure 6.* Self-biasing source-follower. Zin = 10M.**

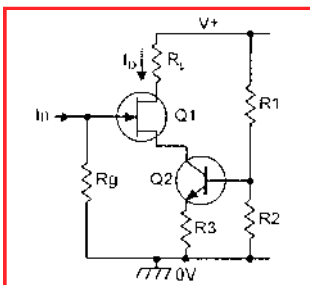


***Figure 5.* Basic JFET 'constant-current' biasing system.**

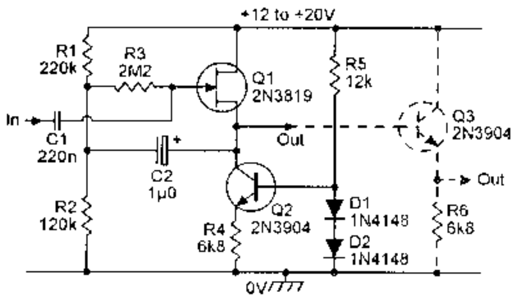


Figure 8. **Hybrid source follower. Zin = 500M.**

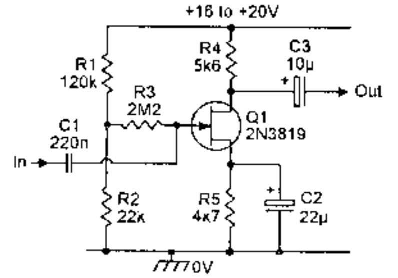


Figure 12. **Common-source amplifier with offset gate biasing.**

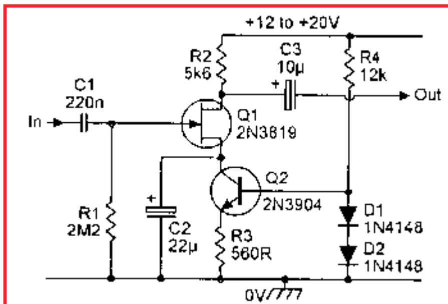


Figure 13. **'Hybrid' common-source amplifier.**

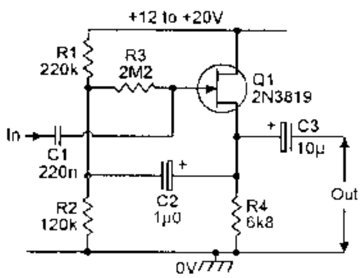


Figure 7. **Source follower with offset biasing. Zin = 44M.**

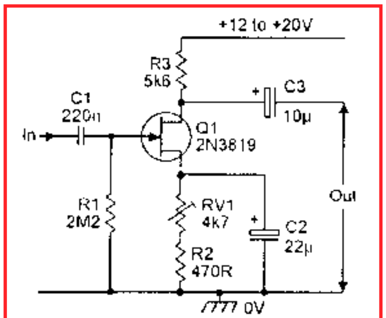


Figure 9. **Simple self-biasing common-source amplifier.**

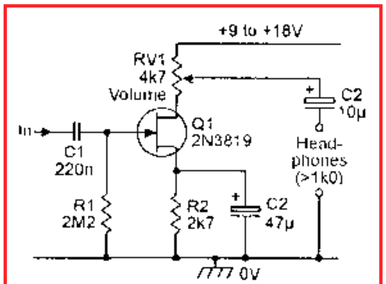


Figure 10. **Simple headphone amplifier.**

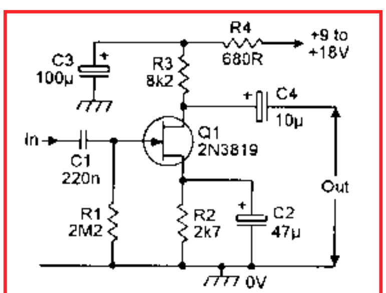


Figure 11. **General-purpose add-on pre-amplifier.**

1000M, which is shunted by the JFET's gate impedance; the input impedance of the complete circuit is 500M, shunted by 10pF.

Note then if the high effective value of input impedance of this circuit is to be maintained, the output must either be taken to external loads via an additional emitter follower stage (as shown dotted in the diagram) or must be taken only to fairly high impedance loads.

COMMON SOURCE AMPLIFIERS

Figure 9 shows a simple self-biasing common source amplifier; RV1 is used to set a quiescent 5V6 across R3. The RV1-R2 biasing network is AC-decoupled via C2, and the circuit gives a voltage gain of 21dB (= x12), and has a ±3dB frequency response that spans 15Hz to 250kHz and an input impedance of 2M2 shunted by 50pF. (This high shunt value is due to Miller feedback, which multiplies the JFET's effective gate-to-drain capacitance by the circuit's x12 Av value.)

Figure 10 shows a simple self-biasing headphone amplifier that can be used with headphone impedances of 1k0 or greater. It has a built-in volume control (RV1), has an input impedance of 2M2, and can use any supply in the 9V to 18V range.

Figure 11 shows a self-biasing add-on pre-amplifier that gives a voltage gain in excess of 20dB, has a bandwidth that extends beyond 100kHz, and has an input impedance of 2M2. It can be used with any amplifier that can provide a 9V to 18V power source.

JFET common source amplifiers can — when very high biasing accuracy is needed — be designed using either the 'offset' or 'constant-current' biasing technique. *Figures 12* and *13* show circuits of these types. Note that the 'offset' circuit of *Figure 12* can be used with supplies in the range 16V to 20V only, while the hybrid circuit of *Figure 13* can be used with any supply in the 12V to 20V range. Both circuits give a voltage gain of 21dB, a ±3dB bandwidth of 15Hz to 250kHz, and an input impedance of 2M2.

DC VOLTMETERS

Figure 14 shows a JFET used to make a very simple and basic three-range DC voltmeter with a maximum FSD sensitivity of 0.5V and an input impedance of 11M1. Here, R6-RV2 and R7 form a potential divider across the 12V supply and — if the R7-RV2 junction is used as the circuit's zero-voltage point — sets the top of R6 at +8V and the bottom of R7 at -4V. Q1 is used as a source follower, with its gate grounded via the R1 to R4 network and is offset biased by taking its source to -4V via R5; it consumes about 1mA of drain current.

In *Figure 14*, R6-RV2 and Q1-R5 act as a Wheatstone bridge network, and RV2 is adjusted so that the bridge is balanced and zero current flows in the meter in the absence of an input voltage at Q1 gate. Any voltage applied to Q1 gate then drives the bridge out of balance by a proportional amount, which can be read directly on the meter.

R1 to R3 form a range multiplier network that — when RV1 is correctly adjusted — gives FSD ranges of 0.5V, 5V, and 50V. R4 protects Q1's gate against damage if excessive input voltage is applied to the circuit.

To use the *Figure 14* circuit, first trim RV2 to give zero meter reading in the absence of an input voltage, and then connect an accurate 0.5V DC to the input and trim RV1 to give a precise full-scale meter reading. Repeat these adjustments until consistent zero and full-scale readings are obtained; the unit is then ready for use.

In practice, this very simple circuit tends to drift with variations in supply voltage and temperature, and fairly frequent trimming of the zero control is needed. Drift can be greatly reduced by using a zener-stabilized 12V supply.

Figure 15 shows an improved low-drift version of the JFET voltmeter. Q1 and Q2 are wired as a differential amplifier, so any drift occurring on one side of the circuit is automatically countered by a similar drift on the other side, and good stability is obtained. The circuit uses the 'bridge' principle, with Q1-R5 forming one side of the bridge and Q2-R6 forming the other. Q1 and Q2 should ideally be a matched pair of JFETs, with IDSS

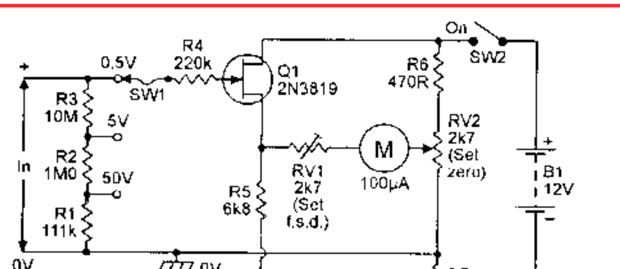
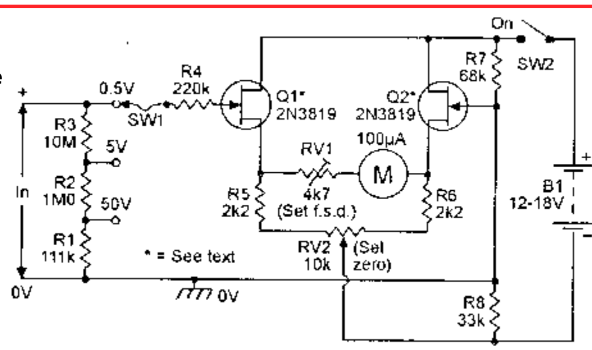


Figure 14. **Simple three-range DC voltmeter.**

Figure 15. **Low-drift three-range DC voltmeter.**



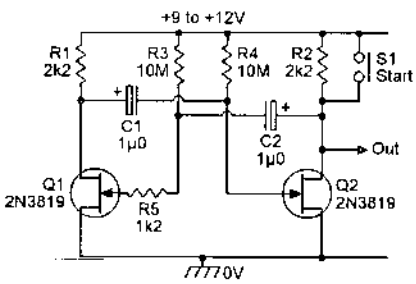


***Figure 16*. VLF astable multivibrator.**

values matched within 10%. The circuit is set up in the same way as that of *Figure 14*.

MISCELLANEOUS JFET CIRCUITS

To conclude this month's article, *Figures 16* to *19* show a miscellaneous collection of useful JFET circuits. The *Figure 16* design is that of a very-low-frequency (VLF) astable or free-running multivibrator; its on and off periods are controlled by C1-R4 and C2-R3, and R3 and R4 can have values up to 10M.

With the values shown, the circuit cycles at a rate of once per 20 seconds, i.e., at a frequency of 0.05Hz; start button S1 must be held closed for at least one second to initiate the astable action.

Figure 17 shows — in basic form — how a JFET and a 741 op-amp can be used to make a voltage-controlled amplifier/attenuator. The op-amp is used in the inverting mode, with its voltage gain set by the R2/R3 ratio, and R1 and the JFET are used as a voltage-controlled input attenuator.

When a large negative control voltage is fed to Q1 gate, the JFET acts like a near-infinite resistance and causes zero signal attenuation, so the circuit gives high overall gain but, when the gate bias is zero, the FET acts like a low resistance and causes heavy signal attenuation, so the circuit gives an overall signal loss.

Intermediate values of signal attenuation and overall gain or loss can be obtained by varying the control voltage value.

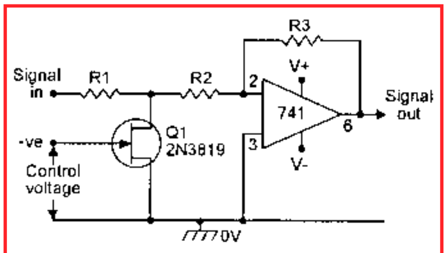


***Figure 17*. Voltage-controlled amplifier/attenuator.**

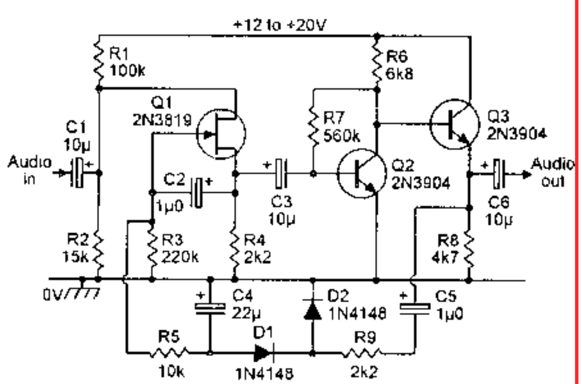
Figure 18 shows how this voltage-controlled attenuator technique can be used to make a 'constant volume' amplifier that produces an output signal level change of only 7.5dB when the input signal level is varied over a 40dB range (from 3mV to 300mV RMS).

The circuit can accept input signal levels up to a maximum of 500mV RMS Q1 and R4 are wired in series to form a voltage-controlled attenuator that controls the input signal level to common emitter amplifier Q2, which has its output buffered via emitter follower Q3.

Q3's output is used to generate (via C5-R9-D1-D2-C4-R5) a DC control voltage that is fed back to Q1's gate, thus forming a DC negative-feedback loop that automatically adjusts the overall voltage gain so that the output signal level tends to remain constant as the input signal level is varied, as follows.

When a very small input signal is applied to the circuit, Q3's output signal is also small, so negligible DC control voltage is fed to Q1's gate; Q1 thus acts as a low resistance under this condition, so almost the full input signal is applied to Q2 base, and the circuit gives high overall gain.

***Figure 18*. Constant-volume amplifier.**



When a large input signal is applied to the circuit, Q3's output signal tends to be large, so a large DC negative control voltage is fed to Q1's gate; Q1 thus acts as a high resistance under this condition, so only a small part of the input signal is fed to Q2's base, and the circuit gives low overall gain.

Thus, the output level stays fairly constant over a wide range of input signal levels; this characteristic is useful in cassette recorders, intercoms, and telephone amplifiers, etc.

Finally, *Figure 19* shows a JFET used to make a DC-to-AC converter or 'chopper' that produces a square-wave output with a peak amplitude equal to that of the DC input voltage.

In this case, Q1 acts like an electronic switch that is wired in series with R1 and is gated on and off at a 1kHz rate via the Q2-Q3 astable circuit, thus giving the DC-to-AC conversion. Note that Q1's gate-drive signal amplitude can be varied via RV1; if too large a drive is used, Q1's gate-to-source junction starts to avalanche, causing a small spike voltage to break through the drain and give an output even when no DC input is present.

To prevent this, connect a DC input and then trim RV1 until the output is just on the verge of decreasing; once set up in this way, the circuit can be reliably used to chop voltages as small as a fraction of a millivolt. **NV**

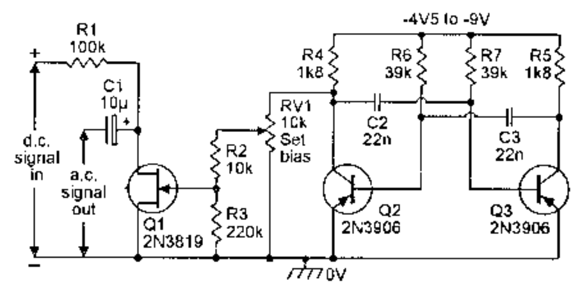


***Figure 19*. DC-to-AC converter or 'chopper' circuit.**

FET PRINCIPLES AND CIRCUITS Part 3

Field-Effect Transistors

by Ray Marston

Ray Marston looks at practical MOSFET and CMOS circuits in this penultimate episode of this four-part series.

Part 1 of this series explained (among other things) the basic operating principles of the MOSFET (or IGFET), and pointed out that complementary enhancement-mode pairs of these devices form the basis of the digital technology known as CMOS.

The present episode of the series looks at practical applications of MOSFETs and CMOS-based MOSFET devices.

A MOSFET INTRODUCTION

MOSFETs are available in both depletion-mode and enhancement-mode versions. Depletion-mode types give a performance similar to a JFET, but with a far higher input resistance (i.e., with a far higher low-frequency input impedance).

Some depletion-mode MOSFETs are equipped with two independent gates, enabling the drain-to-source currents to be controlled via either one or both of the gates; these devices (which are often used as signal mixers in VHF tuners) are known as dual-gate or tetrode MOSFETs, and use the symbol shown in *Figure 1*.

Most modern MOSFETs are enhancement-mode devices, in which the drain-to-source conduction channel is closed when the gate bias is zero, but can be opened by applying a forward gate bias. This 'normally open-circuit' action is implied by the gaps between source and drain in the device's standard symbol, shown in *Figure 2(a)*, which depicts an n-channel MOSFET (the arrow head is reversed in a p-channel device). In some devices, the semiconductor substrate is made externally available, creating a 'four-terminal' MOSFET, as shown in *Figure 2(b)*.

***Figure 1.* Symbol of the dual-gate or tetrode MOSFET.**

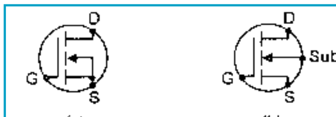


***Figure 2.* Standard symbols of (a) three-pin and (b) four-pin n-channel enhancement-mode MOSFETs.**

Figure 3 shows typical transfer characteristics of an n-channel enhancement-mode MOSFET, and *Figure 4* shows the V_{GS}/I_D curves of the same device when powered from a 15V supply. Note that no significant I_D current flows until the gate voltage rises to a threshold (V_{TH}) value of a few volts but that, beyond this value, the drain current rises in a non-linear fashion.

Also note that the *Figure 3* graph is divided into two characteristic regions, as indicated by the dotted line; these being the 'triode' region, in which the MOSFET acts like a voltage-controlled resistor, and the 'saturated' region,' in which it acts like a voltage-controlled constant-current generator.

Because of their very high input resistances, MOSFETs are vulnerable to damage via electrostatic discharges; for this reason, MOSFETs are sometimes provided with integral protection via diodes or zeners.

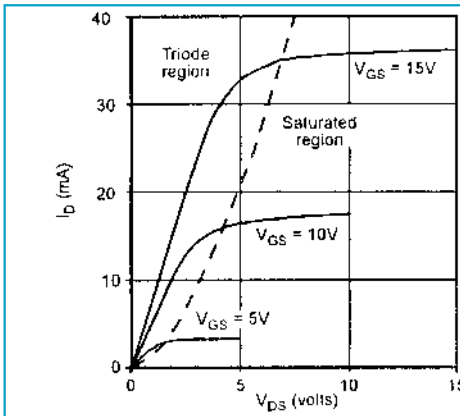


***Figure 3.* Typical transfer characteristics of 4007UB n-channel enhancement-mode MOSFETs.**

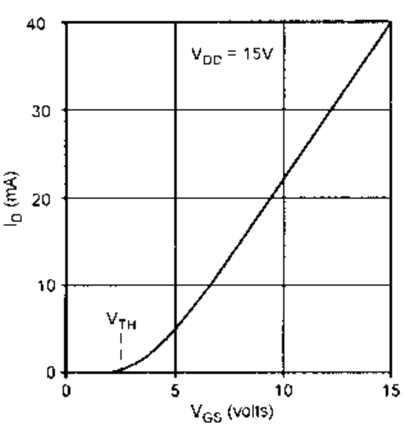


***Figure 4.* Typical V_{GS}/I_D characteristics of 4007UB n-channel enhancement-mode MOSFET.**

THE 4007UB

The easiest and cheapest practical way of learning about enhancement-mode MOSFETs is via a 4007UB IC, which is the simplest member of the popular CMOS '4000-series' digital IC range, and actually houses six useful MOSFETs in a single 14-pin DIL package.

Figure 5 shows the functional diagram and pin numbers of the 4007UB, which houses two complementary pairs of independently-accessible MOSFETs and a third complementary MOSFET pair that is connected as a standard CMOS inverter stage.

Each of the IC's three independent input terminals is internally connected to the standard CMOS protection network shown in *Figure 6*.

Within the IC, Q1, Q3, and Q5 are p-channel MOSFETs, and Q2, Q4, and Q6 are n-channel types. Note that the performance graphs of *Figures 3* and *4* actually apply to the individual n-channel devices within this CMOS IC.

The 4007UB usage rules are simple. In any given application, all unused IC elements must be disabled. Complementary pairs of MOSFETs can be disabled by connecting them as standard CMOS inverters (i.e., gate-to-gate and source-to-source) and tying their inputs to ground, as shown in *Figure 7*.

Individual MOSFETs can be disabled by tying their source to their substrate and leaving the drain open circuit. In use, the IC's input terminal must not be allowed to rise above V_{DD} (the supply voltage) or fall below V_{SS} (zero volts).

To use an n-channel MOSFET, the source must be tied to V_{SS}, either directly or via a current-limiting resistor. To use a p-channel MOSFET, the source must be tied to V_{DD}, either directly or via a current-limiting resistor.

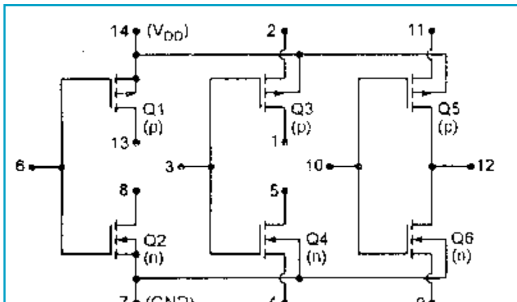


***Figure 5.* Functional diagram of the 4007UB dual CMOS pair plus inverter.**

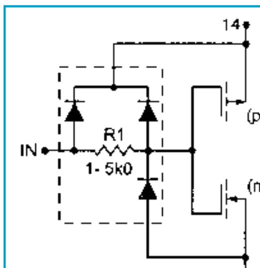


***Figure 6.* Internal-protection network (within dotted lines) on each input of the 4007UB.**

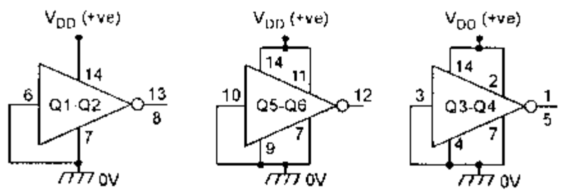


Figure 7. **Individual 4007UB complementary pairs can be disabled by connecting them as CMOS inverters and grounding their inputs.**

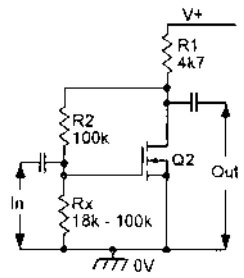


***Figure 8*. Method of biasing n-channel 4007UB MOSFETs for use as a linear inverting amplifier (with medium input impedance).**

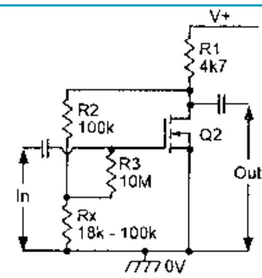


***Figure 9*. High impedance version of the inverting amplifier.**

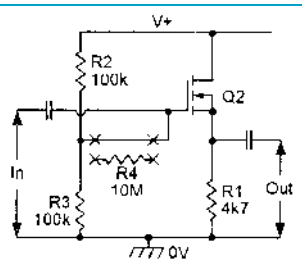


***Figure 10*. Methods of biasing n-channel 4007UB MOSFET as a unity-gain non-inverting amplifier or source follower.**

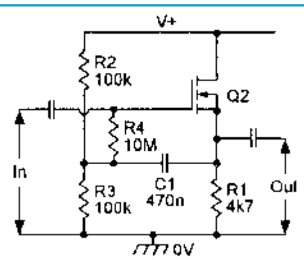


***Figure 11*. Bootstrapped source follower has ultra-high input impedance.**

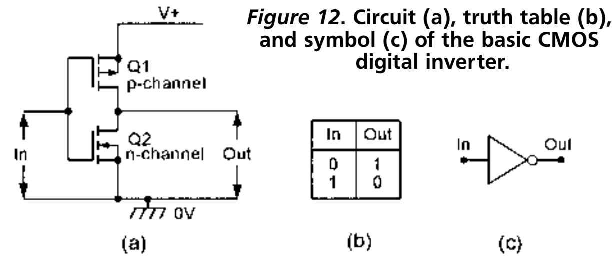


***Figure 12*. Circuit (a), truth table (b), and symbol (c) of the basic CMOS digital inverter.**

LINEAR OPERATION

To fully understand the operation and vagaries of CMOS circuitry, it is necessary to understand the linear characteristics of basic MOSFETs, as shown in the graph of *Figure 4*.

Note that negligible drain current flows until the gate rises to a 'threshold' value of about 1.5 to 2.5 volts, but that the drain current then increases almost linearly with further increases in gate voltage.

Figure 8 shows how to use an n-channel 4007UB MOSFET as a linear inverting amplifier. R1 acts as Q2's drain load, and R2-Rx bias the gate so that Q2 operates in the linear mode.

The Rx value is selected to give the desired quiescent drain voltage, and is normally in the 18k to 100k range.

The amplifier can be made to give a very high input impedance by wiring a 10M isolating resistor between the R2-Rx junction and Q2 gate, as shown in *Figure 9*.

Figure 10 shows how to use an n-channel MOSFET as a unity-gain non-inverting common-drain amplifier or source follower.

The MOSFET gate is biased at half-supply volts by the R2-R3 divider, and the source terminal automatically takes up a quiescent value that is slightly more than V_{TH} below the gate value.

The basic circuit has an input impedance equal to the paralleled values of R2 and R3 (=50k), but can be increased to greater than 10M by wiring R4 as shown.

Alternatively, the input impedance can be raised to several hundred megohms by bootstrapping R4 via C1 as shown in *Figure 11*.

Note from the above description that the enhancement-mode MOSFET performs like a conventional bipolar transistor, except that it has an ultra-high input impedance and has a substantially larger input-offset voltage (the base-to-emitter offset of a bipolar is typically 600mV, while the gate-to-source offset voltage of a MOSFET is typically two volts).

Allowing for these differences, the enhancement-mode MOSFET can thus be used as a direct replacement in many small-signal bipolar transistor circuits.

THE CMOS INVERTER

A major application of enhancement-mode MOSFETs is in the basic CMOS inverting stage of *Figure 12(a)*, in which an n-channel and a p-channel pair of MOSFETs are wired in series but share common input and output terminals.

This basic CMOS circuit is primarily meant for use in digital applications (as described towards the end of Part 1 of this series), in which it consumes negligible quiescent current but can source or sink substantial output currents.

Figures 12(b) and *12(c)* show the inverter's digital truth table and its circuit symbol. Note that Q5 and Q6 of the 4007UB IC are fixed-wired in the CMOS inverter configuration.

Although intended primarily for digital use, the basic CMOS inverter can be used as a linear amplifier by biasing its input to a value between the logic-0 and logic-1 levels; under this condition Q1 and Q2 are both biased partly on, and the inverter thus passes significant quiescent current.

Figure 13 shows the typical drain-current (I_D) transfer characteristics of the circuit under this condition; I_D is zero when the input is at zero or full supply volts, but rises to a maximum value (typically 0.5mA at 5V, or 10.5mA at 15V) when the input is at roughly half-supply volts, under which condition both MOSFETs of the inverter are biased equally.

Figure 14 shows the typical input-to-output voltage-transfer characteristics of the simple CMOS inverter at different supply voltage values. Note that the output voltage changes by only a small amount when the input voltage is shifted around the V_{DD} and 0V levels, but that when V_{in} is biased at roughly half-supply volts, a small change of input voltage causes a large change of output voltage.

Typically, the inverter gives a voltage gain of about 30dB when used with a 15V supply, or 40dB at 5V.

Figure 15 shows a practical linear CMOS inverting amplifier stage. It is biased by wiring 10M resistor R1 between the input and output terminals, so that the output self-biases at approximately

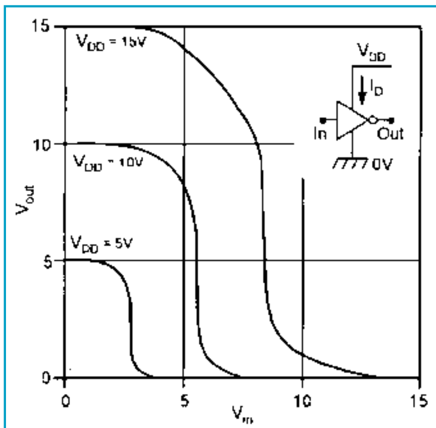


***Figure 14*. Typical input-to-output voltage transfer characteristics of the 4007UB simple CMOS inverter.**

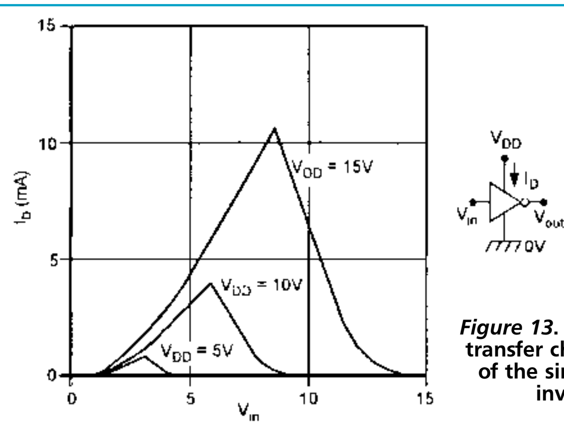


***Figure 13*. Drain-current transfer characteristics of the simple CMOS inverter.**

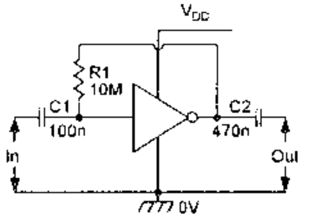


***Figure 15.* Method of biasing the simple CMOS inverter for linear operation.**

half-supply volts.

Figure 16 shows the typical voltage gain and frequency characteristics of this circuit when operated at three alternative supply rail values; this graph assumes that the amplifier output is feeding into the high impedance of a 10M/15pF oscilloscope probe and, under this condition, the circuit has a bandwidth of 2.5MHz when operating from a 15V supply.

As would be expected from the voltage transfer graph of *Figure 14*, the distortion characteristics of the CMOS linear amplifier are quite good with small-amplitude signals (output amplitudes up to 3V peak-to-peak with a 15V supply), but the distortion then increases as the output approaches the upper and lower supply limits. Unlike a bipolar transistor circuit, the CMOS amplifier does not 'clip' excessive sinewave signals, but progressively rounds off their peaks.

Figure 17 shows the typical drain-current versus supply-voltage characteristics of the CMOS linear amplifier. The current typically varies from 0.5mA at 5V, to 12.5mA at 15V.

In many applications, the quiescent supply current of the 4007UB CMOS amplifier can be usefully reduced — at the cost of reduced amplifier bandwidth — by wiring external resistors in series with the source terminals of the two MOSFETs of the CMOS stage, as shown in the 'micropower' circuit of *Figure 18*.

This diagram also lists the effects that different resistor values have on the drain current, voltage gain, and bandwidth of the amplifier when operated from a 15V supply and with its output loaded by a 10M/15pF oscilloscope probe.

Note that the additional resistors of the *Figure 18* circuit increase the output impedance of the amplifier (the output impedance is roughly equal to the R1-A_V product), and this impedance and the external load resistance/capacitance has a great effect on the overall gain and bandwidth of the circuit.

When using a 10k value for R1, for example, if the load capacitance is increased (from 15pF) to 50pF, the bandwidth falls to about 4kHz, but if the capacitance is reduced to 5pF, the bandwidth increases to 45kHz. Similarly, if the resistive load is reduced from 10M to 10k, the voltage gain falls to unity; for significant gain, the load resistance must be large relative to the output impedance of the amplifier.

The basic (unbiased) CMOS inverter stage has an input capacitance of about 5pF and an input resistance of near-infinity. Thus, if the output of the *Figure 18* circuit is fed directly to such a load, it shows a voltage gain of x30 and a bandwidth of 3kHz when R1 has a value of 1M0; it even gives a useful gain and bandwidth when R1 has a value of 10M, but consumes a quiescent current of only 0.4µA.

PRACTICAL CMOS

The CMOS linear amplifier can easily be used in either its standard or micropower forms to make a variety of fixed-gain amplifiers, mixers, integrators, active filters, and oscillators, etc. A selection of such circuits is shown in *Figures 19* to *23*.

Figure 19 shows the practical circuit of an x10 inverting amplifier. The CMOS stage is biased by feedback resistor R2, and the voltage gain is set at x10 by the R1/R2 ratio. The input impedance of the circuit is 1M0, and equals the R1 value.

Figure 20 shows the above circuit modified for use as an audio 'mixer' or analog voltage adder. The circuit has four input terminals, and the voltage gain between each input and the output is fixed at unity by the relative values of the 1M0 input resistor and the 1M0 feedback resistor.

Figure 21 shows the basic CMOS amplifier used as a simple integrator.

Figure 22 shows the linear CMOS amplifier used as a crystal oscillator. The amplifier is linearly biased via R1 and provides 180° of phase shift at the crystal resonant frequency, thus enabling the circuit to oscillate. If the user wants the crystal to provide a frequency accuracy within 0.1% or so, Rx can be replaced by a short and C1-C2 can be omitted. For ultra-high accuracy, the correct values of Rx-C1-C2 must be individually determined (the diagram shows the typical range of values).

Finally, *Figure 23* shows a 'micropower' version of the CMOS crystal oscillator. In this case, Rx is actually incorporated in the amplifier. If desired, the output of this oscillator can be fed directly to the input of an additional CMOS inverter stage, for improved waveform shape/amplitude. **NV**

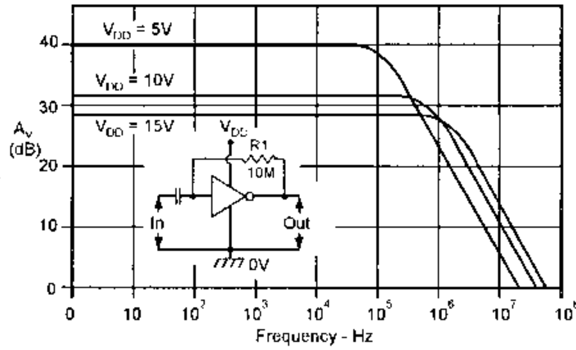


***Figure 16.* Typical A_V and frequency characteristics of the linear-mode basic CMOS amplifier.**

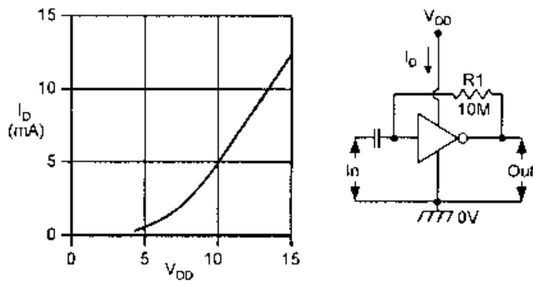
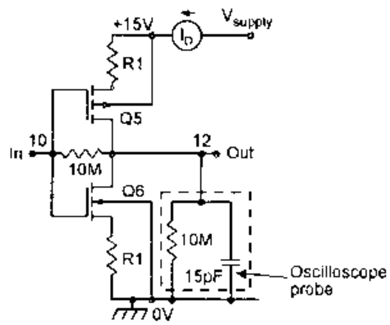


***Figure 17.* Typical I_D/V_{DD} characteristics of the linear-mode CMOS amplifier.**



R1	I_D	A_V (V_{out}/V_{in})	Upper 3dB Bandwidth
0	12.5mA	20	2.7MHz
100R	8.2mA	20	1.5MHz
560R	3.9mA	25	300kHz
1k0	2.5mA	30	150kHz
5k6	600µA	40	25kHz
10k	370µA	40	15kHz
100k	40µA	30	2kHz
1M0	4µA	10	1kHz

***Figure 18.* Micropower 4007UB CMOS linear amplifier, showing method of reducing I_D, with performance details.**

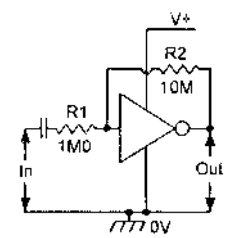


***Figure 19.* Linear CMOS amplifier wired as x10 inverting amplifier.**

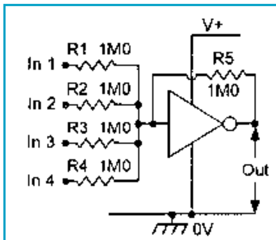


***Figure 20.* Linear CMOS amplifier wired as unity-gain four-input audio mixer.**

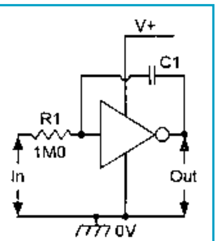


***Figure 21.* Linear CMOS amplifier wired as an integrator.**

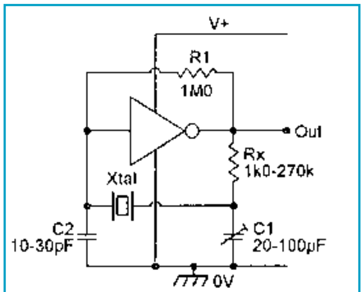


***Figure 22.* Linear CMOS amplifier wired as a crystal oscillator.**

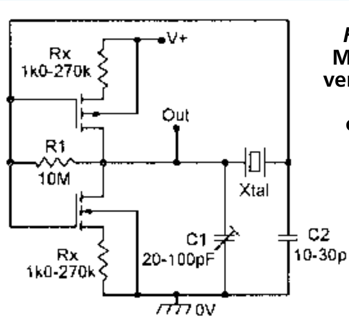


***Figure 23.* Micropower version of the crystal oscillator.**

FET PRINCIPLES AND CIRCUITS — Part 4

Field-Effect Transistors

by Ray Marston

Ray Marston looks at practical VMOS power FET circuits in this final episode of this four-part series.

Part 1 of this series explained (among other things) the basic operating principles of those enhancement-mode power-FET devices known as VFETs or VMOS. This final episode of the series takes a deeper look at these devices and shows practical ways of using them.

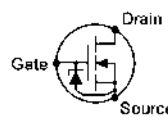


***Figure 1.* Symbol of Siliconix VMOS power FET with integral zener diode gate protection.**

Device type number	P_{TOT} (max) (W)	I_D (max) (A)	V_{DS} (max) (V)	V_{GS} (max) (V)	V_{TH} (min-max) (V)	g_m (typ) (mmho)	C_{IN} (max) (pF)	f_T (typ) (MHz)
VN10KM	1	0.5	60	5	0.3 - 2.5	200	48	–
VN1010	1	0.5	100	15	2V max	200	48	–
VN48AF	12.5	2	40	15	0.8 - 2	250	50	600
VN66AF	12.5	2	60	15	0.8 - 2	250	50	600
VN88AF	12.5	2	80	15	0.8 - 2	250	50	600

***Figure 2.* Major parameters of five popular n-channel Siliconix VMOS power FETs.**

A VMOS INTRODUCTION

A VFET can, for most practical purposes, be simply regarded as a high-power version of a conventional enhancement-mode MOSFET. The specific form of VFET construction shown in *Figure 17* in Part 1 of this series was pioneered by Siliconix in the mid-1970s, and the devices using this construction are marketed under the trade name 'VMOS power FETs' (Vertically-structured Metal-Oxide Silicon power Field-Effect Transistors). This 'VMOS' name is traditionally associated with the V-shaped groove formed in the structure of the original (1976) versions of the device.

Siliconix VMOS power FETs are probably the best known type of VFETs. They are available as n-channel devices only, and usually incorporate an integral zener diode which gives the gate a high degree of protection against accidental damage; *Figure 1* shows the standard symbol used to represent such a device, and *Figure 2* lists the main characteristics of five of the most popular members of the VMOS family; note in particular the very high maximum operating frequencies of these devices.

Other well-known families of 'Vertically-structured' power MOSFETS are those produced by Hitachi, Supertex, and Farranti, etc. Some of these V-type power MOSFETs are available in both n-channel and p-channel versions and are useful in various high-performance complementary audio power amplifier applications.

THE VN66AF

The best way to get to know VMOS is to actually 'play' with it, and the readily available Siliconix VN66AF is ideal for this purpose. It is normally housed in a TO202-style plastic-with-metal-tab package with the outline and pin connections shown in *Figure 3*.

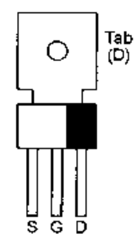


***Figure 3.* Outline and pin connections of the TO202-cased VN66AF power FET.**

Figure 4 lists the major static and dynamic characteristics of the VN66AF. Points to note here are that the input (gate-to-source) signal must not exceed the unit's 15V zener rating, and that the device has a typical dynamic input capacitance of 50pF. This capacitance dictates the dynamic input impedance of the VN66AF; the static input impedance is of the order of a million megohms. *Figures 5* and *6* show the VN66AF's typical output and saturation characteristics. Note the following specific points from these graphs.

(1) The device passes negligible drain current until the gate voltage reaches a threshold value of about 1V; the drain current then increases non-linearity as the gate is varied up to about 4V, at which point the drain current value is about 400mA; the device has a square-law transfer characteristic below 400mA.

(2) The device has a highly linear transfer characteristic above 400mA (4V on the gate) and thus offers good results as a low-distortion class-A power amplifier.

(3) The drain current is controlled almost entirely by the gate voltage and is almost independent of the drain voltage so long as the device is not saturated. A point not shown in the diagram is that, for a given value of gate voltage, the drain current has a negative temperature coefficient of about 0.7% per °C, so that the drain current decreases as temperature rises. This characteristic gives a fair degree of protection against

STATIC	Max drain-to-source voltage	60V
	Max drain-to-gate voltage	60V
	Max continuous drain current	2A
	Max pulsed drain current	3A
	Max continuous forward gate current	2mA
	Max pulsed forward gate current	100mA
	Max continuous reverse gate current	100mA
	Max reverse gate-to-source (zener) voltage	15V
	Max dissipation at 25°C case temperature	15W
	Gate threshold voltage	0.8V min, 2.0A typ.
	Zero-gate-voltage drain current at 25°C	10µA max
	On-state drain current at V_{GS} = 10V	1.0A min, 2.0A typ.
	Temperature operating and storage range	-40 to +150°C
DYNAMIC	Forward transconductance (typical)	250 mmho
	Input capacitance (typical)	50pF
	Reverse transfer capacitance (typical)	10pF
	Common-source output capacitance (typical)	50pF
	Typical switching times, 25V supply, 23R load, 0-10V gate drive from a 50R source: Turn-on delay	2nS
	Rise time	2nS
	Turn-off delay	2nS
	Fall time	2nS

***Figure 4.* Major static and dynamic characteristics of the VN66AF.**

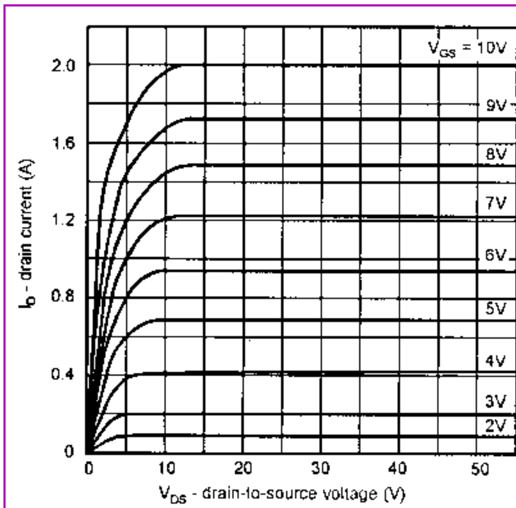


***Figure 5.* Typical output characteristics of the VN66AF.**

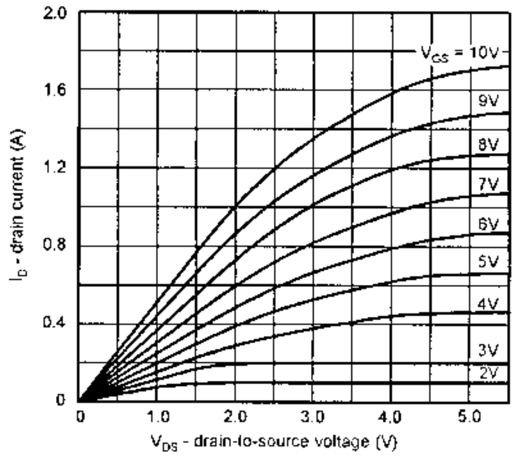


Figure 6. **Typical saturation characteristics of the VN66AF.**

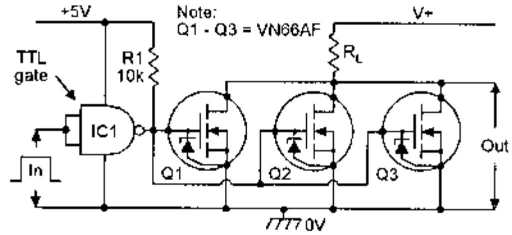


Figure 10. **Method of boosting the output of *Figure 9* by driving three VN66AFs in parallel.**

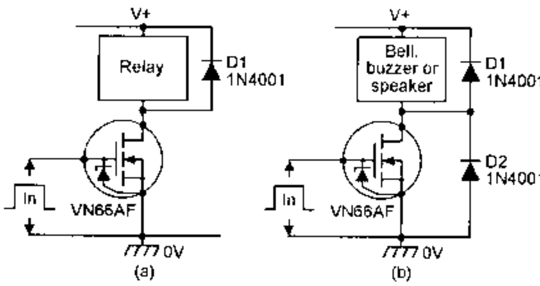


Figure 11. **If inductive loads such as relays (a) or bells, buzzers, or speakers (b) are used in digital switching circuits, protection diodes must be wired as shown.**

thermal runaway.

(4) When the device is saturated (switched fully on) the drain-to-source path acts as an almost pure resistance with a value controlled by the gate voltage. The resistance is typically 2R0 when 10V is on the gate, and 10R when 2V is on the gate. The device's 'off' resistance is in the order of megohms. These features make the device highly suitable for use as a low-distortion high-speed analog power switch.

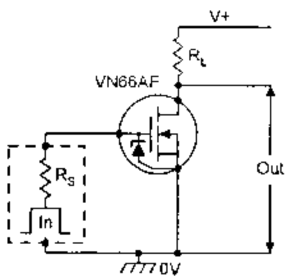


Figure 7. **Basic VMOS digital switch or amplifier.**

DIGITAL CIRCUITS

VMOS can be used in a wide variety of digital and analog applications. It is delightfully easy to use in digital switching and amplifying applications; *Figure 7* shows the basic connections. The load is wired between the drain and the positive supply rail, and the digital input signal is fed directly to the gate terminal. Switch-off occurs when the input goes below the gate threshold value (typically about 1.2V). The drain ON current is determined by the peak amplitude of the gate signal, as shown in *Figure 5*, unless saturation occurs. In most digital applications, the ON current should be chosen to ensure saturation.

The static input impedance of VMOS is virtually infinite, so zero drive power is needed to maintain the VN66AF in the ON or OFF state. Drive power is, however, needed to switch the device from one state to the other; this power is absorbed in charging or discharging the 50pF input capacitance of the VN66AF.

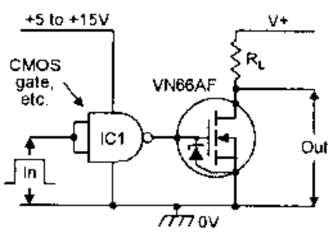


Figure 8. **Methods of driving VMOS from CMOS.**

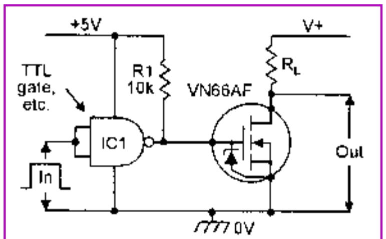


Figure 9. **Method of driving VMOS from TTL.**

The rise and fall times of the output of the *Figure 7* circuit are (assuming zero input rise and fall times) determined by the source impedance of the input signal, by the input capacitance and forward transconductance of the VMOS device, and by the value of R_L. If R_L is large compared to R_S, the VN66AF gives rise and fall times of roughly 0.11nS per ohm of R_S value. Thus, a 100R source impedance gives a 11nS rise or fall time. If R_L is not large compared to R_S, these times may be considerably changed.

A point to note when driving the VN66AF in digital applications is that its zener forward and reverse ratings must never be exceeded. Also, because of the very high frequency response of VMOS, the device is prone to unwanted oscillations if its circuitry is poorly designed. Gate leads should be kept short, or be protected with a ferrite bead or a small resistor in series with the gate.

VMOS can be interfaced directly to the output of a CMOS IC, as shown in *Figure 8*. Output rise and fall times of about 60nS can be expected, due to the limited output currents available from a single CMOS gate, etc. Rise and fall times can be reduced by driving the VMOS from a number of CMOS gates wired in parallel, or by using a special high-current driver.

VMOS can be interfaced to the output of TTL by using a pull-up resistor on the TTL output, as shown in *Figure 9*. The 5V TTL output of this circuit is sufficient to drive 600mA through a single VN66AF. Higher output currents can be obtained either by wiring a level-shifter stage between the TTL output and the VMOS input, or by wiring a number of VMOS devices in parallel, as shown in *Figure 10*.

When using VMOS in digital switching applications, note that if inductive drain loads such as relays, self-interrupting bells or buzzers, or moving-coil speakers are used, clamping diodes must be connected as shown in *Figure 11*, to damp inductive back-EMFs and thus protect the VMOS device against damage.

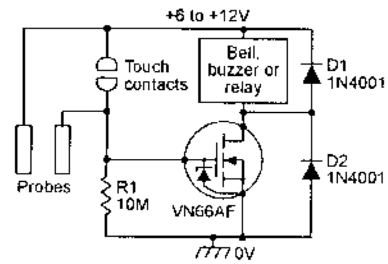


Figure 12. **Water- or touch-activated power switch.**

SOME DIGITAL DESIGNS

Figures 12 to *15* show a few

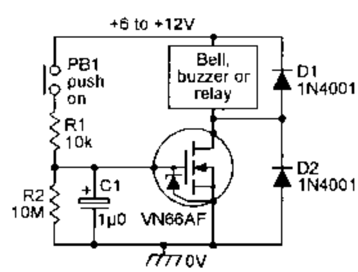


Figure 13. **Delayed-turn-off power switch.**

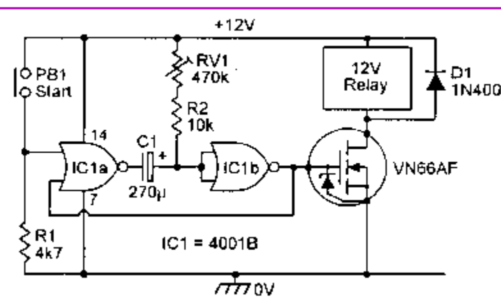


Figure 14. **Simple relay-output timer circuit.**

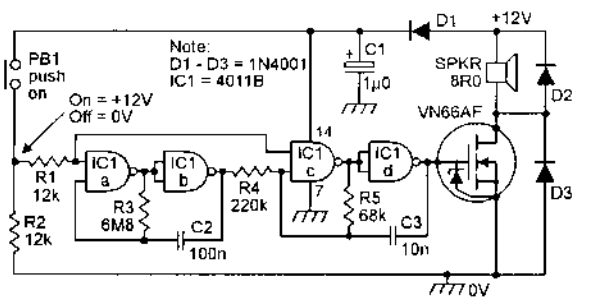


Figure 15. Warble-tone six watt alarm.

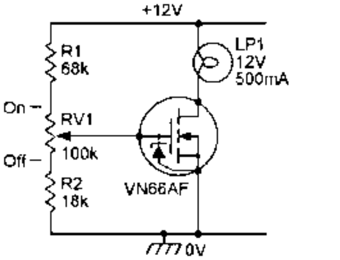


Figure 16. Simple DC lamp dimmer.

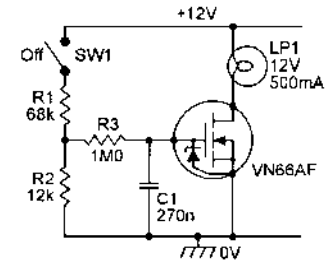


Figure 17. Soft-start lamp switch.

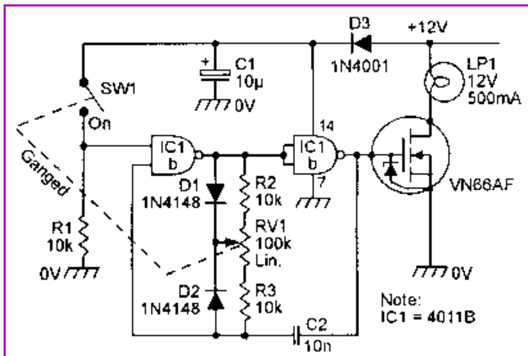
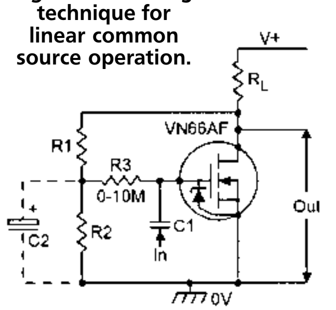


Figure 18. High-efficiency DC lamp dimmer.

Figure 19. Biasing technique for linear common source operation.



simple but useful digital applications of the VN66AF. The water- or touch-activated power switch of *Figure 12* could not be simpler: when the touch contacts and water probes are open, zero volts are on the gate of the VN66AF, so the device passes zero current. When a resistance (zero to 10s of megohms) is placed across the contacts (by contact with skin resistance) or probes (by water contact), a substantial gate voltage is developed by potential divider action and the VN66AF passes a high drain current, thus activating the bell, buzzer, or relay.

In the manually activated delayed-turn-off circuit of *Figure 13*, C1 charges rapidly via R1 when push-button switch PB1 is closed, and discharges slowly via R2 when PB1 is open. The load thus activates as soon as PB1 is closed, but does not deactivate until some 10s of seconds after PB1 is released.

In the simple relay-output timer circuit of *Figure 14*, the VMOS device is driven by the output of a manually triggered monostable or one-shot multivibrator designed around two gates of a 4001B CMOS IC; the relay turns on as soon as PB1 is closed, and then turns off automatically again some pre-set 'delay time' later. The delay is variable from a few seconds to a few minutes via RV1.

Finally, *Figure 15* shows the practical circuit of an inexpensive but very impressive alarm-call generator that produces a 'dee-dah' sound like that of a British police car siren. The alarm can be turned on by closing PB1 or be feeding a 'high' voltage to the R1-R2 junction. The circuit uses an 8R0 speaker and generates roughly six watts of output power.

DC LAMP CONTROLLERS

Figures 16 to *18* show three simple but useful DC lamp controller circuits that can be used to control the brilliance of any 12V lamp with a power rating of up to six watts. A VMOS power FET can, for many purposes, be regarded as a voltage controlled constant-current generator; thus, in *Figure 16*, the VMOS drain current (and thus the lamp brightness) is directly controlled by the variable voltage of RV1's slider. The circuit thus functions as a manual lamp dimmer.

The *Figure 17* circuit is a simple modification of the above design, the action being such that the lamp turns on slowly when the switch is closed as C1 charges up via R3, and turns off slowly when the switch is opened as C1 discharges via R3.

The *Figure 18* circuit is an efficient 'digital' lamp dimmer which controls the lamp brilliance without causing significant power loss across the VMOS device. The two 4011B CMOS gates form an astable multivibrator with a mark/space ratio that is fully variable from 10:1 to 1:10 via RV1; its output is fed to the VN66AF gate, and enables the mean lamp brightness to be varied from virtually fully-off to fully-on. In this circuit, the VMOS device is alternately switched fully on and fully off, so power losses are negligible.

LINEAR CIRCUITS

VMOS power FETs can, when suitably biased, easily be used in either the common source or common drain (voltage follower) linear modes. The voltage gain in the common source mode is equal to the product of R_L and the device's g_M or forward transconductance. In the case of the VN66AF, this gives a voltage gain of 0.25 per ohm of R_L value, i.e., a gain of x4 with a 16R load, or x25 with a 100R load. The voltage gain in the common drain mode is slightly less than unity.

A VMOS power FET can be biased into the linear common source mode by using the standard enhancement-mode MOSFET biasing technique shown in *Figure 19*, in which the R1-R2 potential divider is wired in the drain-to-gate negative feedback loop and sets the quiescent drain voltage at roughly half-supply value, so that maximal signal level swings can be accommodated before clipping occurs.

When — in the *Figure 19* circuit — R3 has a value of zero ohms, the circuit exhibits an input impedance that, because of the AC negative feedback effects, is roughly equal to the parallel values of R1 and R2 divided by the circuit's voltage gain (R_L x g_M. If R3 has a finite value, the input impedance is slightly less than the R3 value, unless AC feedback-decoupling capacitor C2 is fitted in place, in which case, the input impedance is slightly greater than the R3 value.

Figure 20 shows how to bias the VN66AF for common drain (voltage follower) operation. Potential divider R1-R2 sets the VMOS gate at a quiescent value slightly greater than half-supply voltage. When the R3 value is zero, the circuit input impedance is equal to the parallel values of R1 and R2. When the R3 value is finite, the input impedance equals the R3 value plus the parallel R1-R2 values. The input impedance can be raised to a value many times greater than R3 by adding the C2 'bootstrap' capacitor to the circuit.

Finally, *Figure 21* shows a practical example of a VMOS linear application. The circuit is wired as a class-A power amplifier which, because of the excellent linearity of the VN66AF, gives remarkably little distortion for so simple a design. The VN66AF must be mounted on a good heatsink in this application. When the design is used with a purely resistive 8R0 load, the amplifier bandwidth extends up to 10MHz. **NV**

Figure 21. Simple class-A audio power amplifier gives 1% THD at 1W.

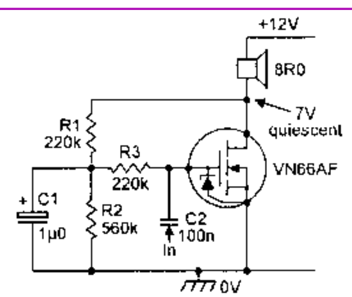


Figure 20. Biasing techniques for linear common drain (voltage follower) operation.