TELEDYNE COMPONENTS

OPERATIONAL AMPLIFIER — FAST-SETTLING, FULLY-DIFFERENTIAL, FET-INPUT

FEATURES

- **Gain-Bandwidth Product.....2000 MHz**
- **Unity-Gain Bandwidth .....80 MHz**
- **Slew Rate @ $A_{CL} = -1$ .....1200 V/µs**
- **Settling Time to 0.01% (10V step).....130 ns**
- **Open Loop Gain .....110 dB**
- **Output .....±13V, ±130 mA**
- **Excellent Low Gain Stability**

APPLICATIONS

- **Video Instrumentation**
- **High-Speed Follower**
- **Low Error Current Integrator**
- **Radar**
- **Video Frequency Filters**
- **Video Line Driver**

GENERAL DESCRIPTION

The 1443's combination of high speed, wide bandwidth, excellent DC characteristics, and low-gain stability places it at the forefront of high-performance operational amplifiers. Its 2 GHz gain-bandwidth product, 1200 V/µs slew rate (when compensated for unity gain), and 130 ns settling time clearly make it an outstanding high-speed device. It has been carefully engineered to eliminate the low-gain stability problems that have historically plagued high-speed op amps such as the BB3554. For example, as a unity-gain follower with a 54 pF capacitive load, the 1443 has a small signal (3 dB) bandwidth of 120 MHz, yet still has 35° of phase margin, without using exotic circuit techniques.

The 1443 has a fully-differential FET input followed by a bipolar gain stage that, together, produce excellent DC characteristics. Common-mode rejection ratio (CMRR) is 80 dB (minimum). Offset voltage and bias current are guaranteed less than ±3 mV and –50 pA, respectively. Open-loop gain is 100 dB (minimum). External compensation with a single capacitor allows users to tailor 1443 performance for different applications.

The 1443 is packaged in an 8-pin TO-3 can and is specified for 0°C to +70°C operation. The 1443 High Reliability (HR) version is specified for –55°C to +125°C operation.

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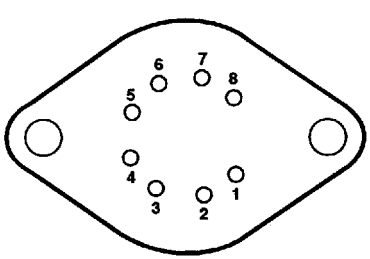
PIN CONFIGURATION

PIN NO.	DESIGNATION
1	OUTPUT
2	$+V_{CC}$
3	COMPENSATION
4	E_{OS} TRIM
5	–INPUT
6	+INPUT
7	$-V_{CC}$
8	E_{OS} TRIM



BOTTOM VIEW

FAST-SETTLING, FULLY-DIFFERENTIAL FET-INPUT OPERATIONAL AMPLIFIER

1443

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ..... ±18V
V_{ID} Differential Input Voltage ..... ±25V
V_{ICM} Common-Mode Input Voltage ..... $\pm V_{CC}$
T_C Operating Temperature Range (Case)
1443 ..... 0°C to +70°C
1443-HR ..... –55°C to +125°C
T_{STG} Storage Temperature Range ..... –65°C to +150°C

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1443 Min	1443 Typ	1443 Max	1443-HR Min	1443-HR Typ	1443-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±1	±3	—	±1	±3	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±25	—	—	±25	±75	µV/°C
I_B	Input Bias Current		—	±10	±50	—	±10	±50	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±5	—	—	±5	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain	R_L = 100Ω	100	110	—	100	110	—	dB
PSRR	Power Supply Rejection Ratio		70	90	—	70	90	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±5V	80	100	—	80	100	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 74 dB	±7	±9	—	±7	±9	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
V_O	Output Voltage Swing	R_L = 100Ω	±10.5	±13	—	±10.5	±13	—	V
I_O	Output Current		±100	±130	—	±100	±130	—	mA
I_{SC}	Output Short-Circuit Current	(Note 2)	—	±160	—	—	±160	—	mA
R_O	Output Resistance (DC Open-Loop)		—	200	—	—	200	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±12	±15	±18	±12	±15	±18	V
I_{CC}	Quiescent Supply Current		—	±45	±55	—	±45	±55	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. The 1443 cannot withstand a continuous short-circuit to ground.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, C_C = short, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1443 Min	1443 Typ	1443 Max	1443-HR Min	1443-HR Typ	1443-HR Max	Unit
S_R	Slew Rate	R_L = 100Ω, A_{CL} = -1	900	1200	—	900	1200	—	V/µs
GBWP	Gain-Bandwidth Product	f = 100 kHz, R_L = 200Ω,	—	2000	—	—	2000	—	MHz
		C_C = 0 pF, f = 1 MHz, R_L = 200Ω, C_C = 10 pF	90	130	—	90	130	—	MHz
UGBW	Unity-Gain Bandwidth		—	80	—	—	80	—	MHz
t_s	Settling Time (A_{CL} = -1)	10V step/1%	—	50	—	—	50	—	ns
		10V step/0.1%	—	80	—	—	80	—	ns
		10V step/0.01%	—	130	165	—	130	165	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	15	—	—	15	—	nV/√Hz
C_L	Capacitive Load (maximum w/o oscillation)	R_L = 100Ω, A_{CL} = -1	—	>300	—	—	>300	—	pF

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

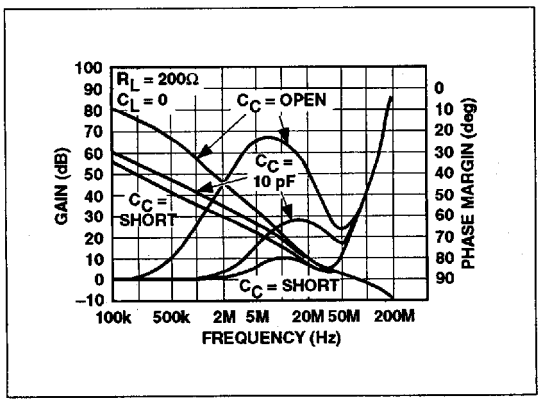


Figure 1. Gain and Phase vs Frequency for Variable Compensation

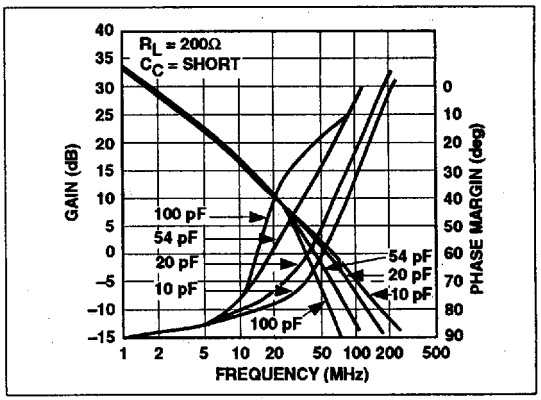


Figure 4. Gain and Phase vs Frequency for Variable C_L

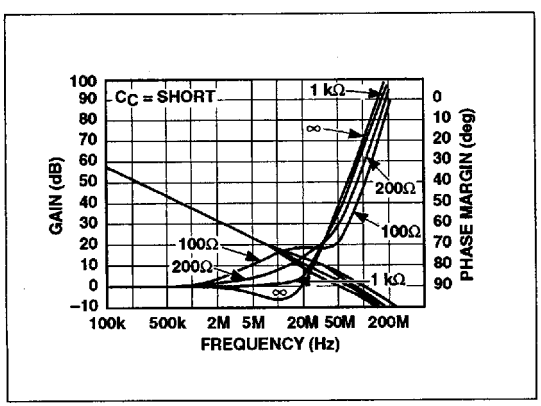
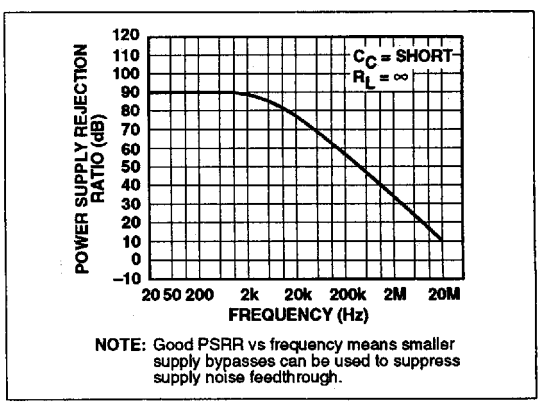


Figure 2. Gain and Phase vs Frequency for Variable R_L



NOTE: Good PSRR vs frequency means smaller supply bypasses can be used to suppress supply noise feedthrough.

Figure 5. PSRR vs Frequency

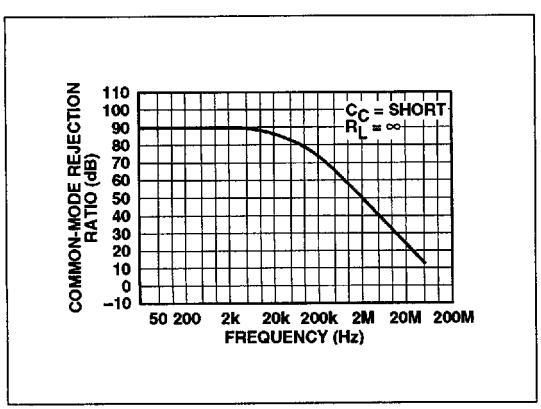


Figure 3. CMRR vs Frequency

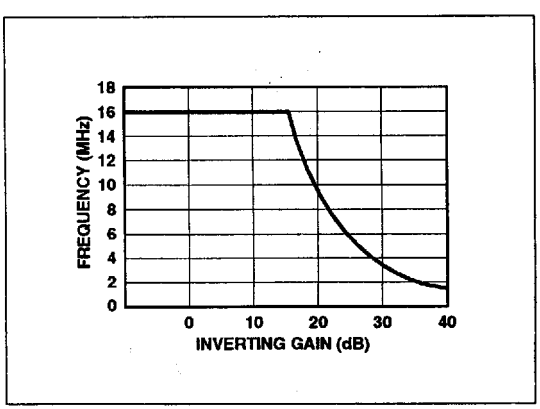


Figure 6. Utilizable Full-Power Bandwidth

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APPLICATIONS INFORMATION

Compensation

The 1443's design allows users to tailor its compensation, and thereby its performance, to suit different applications. The total effective compensation is an internal 5 pF capacitor in series with whatever capacitor is placed between the compensation input (pin 3) and the output (pin 1).

To minimize low frequency (<1 MHz) slewing error and maximize bandwidth for higher gains (>30 dB), the external compensation capacitance should range from 0 pF (open) to 5 pF. For best transient response at lower gains, values greater than 5 pF are recommended. Above approximately 15 pF, a short is recommended in lieu of a larger capacitor. The exact value of compensation depends on how much ringing and overshoot an application allows. Most low-gain applications will achieve best overall results by shorting pin 1 to pin 3.

Following selection of a compensation capacitor (C_C), a feedback capacitor (C_{FB}) must be selected to properly compensate for input capacitance:

$$C_{FB} = 2\ pF/(NG-1),$$

where NG = noise gain.

Noise gain is defined as $1/\beta$, where β is equal to the fraction of the output signal that is fed back to the input. Note that noise gain is the multiple of amplifier input noise which appears at the amplifier output. In case of low C_C, C_{FB} may be increased to provide extra phase lead. The choice of C_{FB} is best made on the basis of permissible overshoot after C_C has been chosen on the basis of gain.

Bypassing

The traditional practice of decoupling power supply lines with bypass capacitors is necessary to prevent high-frequency oscillations resulting from power supply lead inductance and parasitic capacitance. Unfortunately, the bypass capacitor and lead inductance form a tank circuit that can ring when a step change in the op-amp output forces a current pulse from the supply. In many cases, adding a dissipative element (a resistor) will damp the ringing; its exact value is not critical, but its presence is.

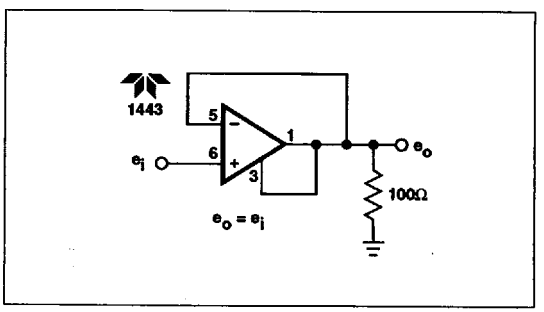
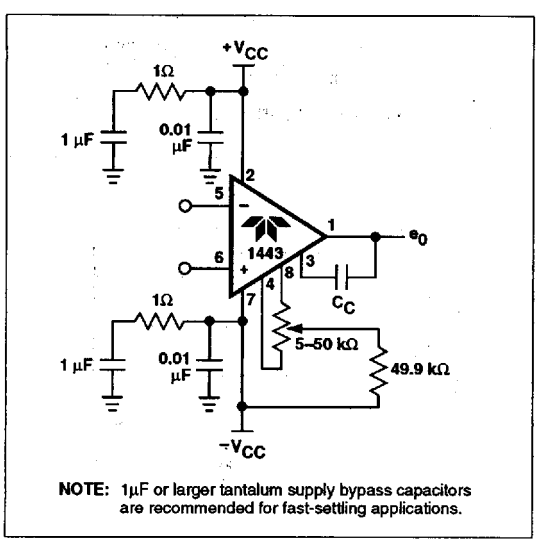


Figure 8. Follower Configuration



NOTE: 1µF or larger tantalum supply bypass capacitors are recommended for fast-settling applications.

Figure 7. Typical Connection

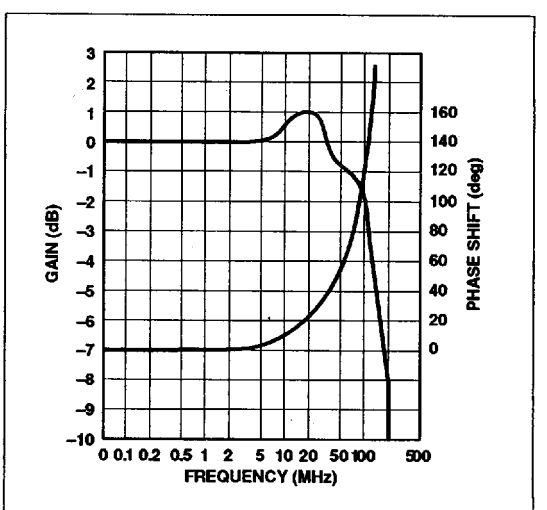


Figure 9. Frequency Response (As a Follower)

Follower

When used as a unity-gain follower (Figure 8), the 1443 has a 3 dB bandwidth of 120 MHz with only 1 dB of peaking, as shown in Figure 9. Pulse response in this configuration is shown in Figure 10.

Unity-Gain Inverter

As a unity-gain inverter (Figure 11), the 1443 has a typical 3 dB bandwidth of 60 MHz. It will settle quickly even with loads of $C_L = 100$ pF and $R_L = 100\Omega$, yet will not oscillate if R_{IN} is open.

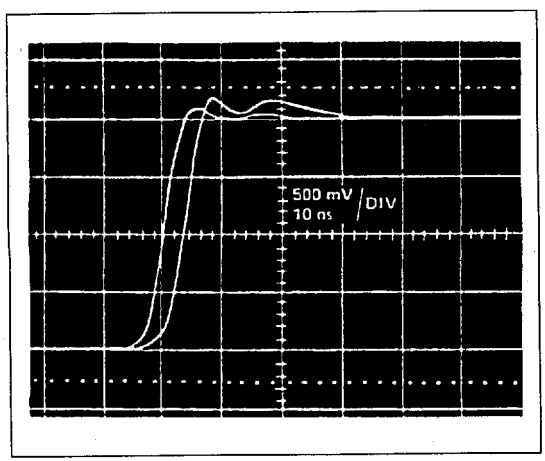


Figure 10. Follower Pulse Response

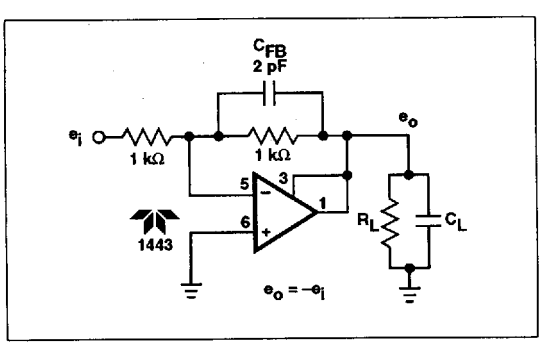


Figure 11. Unity-Gain Inverter

Differential Amplifier

With fully-differential capabilities, the 1443 lends itself to many system configurations. Figure 12 shows a typical configuration for the 1443 as a wideband (approximately 15 MHz) differential amplifier with 20 dB gain.

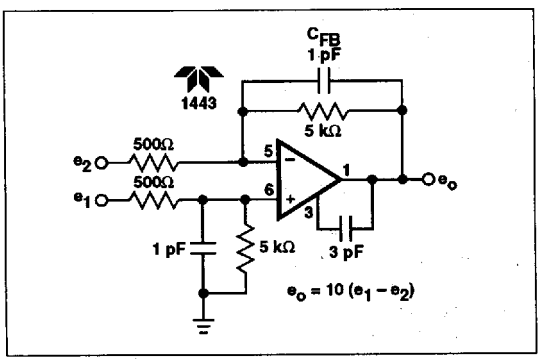


Figure 12. Wideband Differential Amplifier

High-Speed Coaxial Driver

Figure 13 shows the 1443 being used as a high-speed coaxial line driver. The 1443 can drive a 50Ω cable to ±5V with 50Ω terminating resistors at both ends to minimize reflections. Using 1% termination resistors and 50Ω line, ghosts are attenuated at least 77 dB. Without the series 50Ω resistor at the amplifier output, ghosts may only be attenuated by 38 dB.

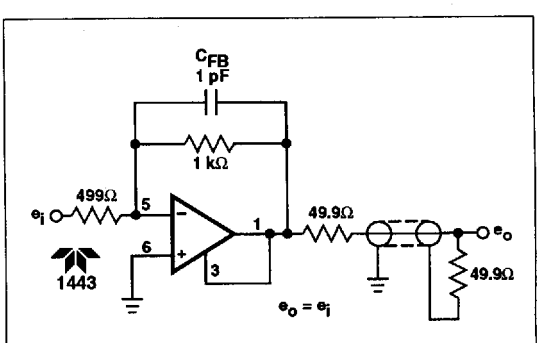


Figure 13. High-Speed Coaxial Driver

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HIGH-FREQUENCY TROUBLESHOOTING TECHNIQUES

Parasitic Oscillations

With VHF operational amplifiers like the 1443, it is not enough to only be concerned with stability problems due to loop closure. Of equal concern (and often times more annoying) are oscillations due to parasitics. Parasitic oscillations are apt to arise in VHF op-amp circuits in which lead lengths are long (>1/2 inch), or loop areas are large (>1 cm^2) at the summing junction, feedback capacitor, power supply pins, or ground-return paths (from bypass capacitors or the amplifier case).

For the 1443, these oscillations may contain frequencies up to 0.5 GHz. Therefore, you cannot always count on seeing them with an oscilloscope. When parasitic oscillation occurs, it often appears as a DC offset because circuit conductance nonlinearities detect its RF envelope. If what appears to be a DC offset is noisy and erratic, or responsive to the placement of your finger or a test probe, parasitic oscillations may be the problem.

Parasitic oscillations are also likely if there is any significant lead length separating the amplifier output from its load capacitance. The lead inductance and load capacitance form a series LC circuit that looks like a larger and larger capacitor as it approaches resonant frequency from below.

Even lead lengths associated with attaching an oscilloscope probe can cause problems. For a typical scope probe, with the ground attached 10 cm from the measurement point, the ground lead and probe form a series LC circuit of approximately 100 nH and 12 pF. At 100 MHz band-edge for the 1443, the apparent probe capacitance will double. In parallel with already-existing circuit capacitances, this 24 pF may be enough to cause oscillation. A good practice is to wrap the ground lead around the probe tip. An even better practice is to use a probe socket (Tektronix 131-0258-00) installed in the circuit, with careful choice of the ground return route.

Semiconductor capacitances and bandwidths are nonlinearly-dependent on voltage and current. Devices that oscillate at one voltage level may not oscillate at another. Check for op-amp oscillations at zero volt output and at several additional output points in each polarity. You will often find that oscillations exist at one or two points in the circuits' output range. These might be observed only as unexplained perturbations on the output (they may not appear as bursts) due to envelope detection, as previously discussed.

The Finger as an Analog Development Tool

In 15V systems, the finger can be a useful investigative tool, if thoughtfully applied. It can couple signals in and out and can also be used as a load. A well-laid-out RF op-amp circuit will be only slightly affected by a light touch. Dramatic changes reveal a sensitive point! Check a circuit by touching the amplifier case, the supply rails (carefully), ground, control knobs, chassis parts, etc. If things change markedly when you touch these areas, parasitics may be the problem.

Other Considerations

Problems commonly associated with video amplifiers are naturally present in VHF circuits. Therefore, proper compensation of input capacitance by C_{FB} cannot be ignored. Nor can the impedance (inductance) of the ground return paths (though use of a ground-plane is helpful, it is no panacea).

Thermal Considerations

The 1443 has internal current limiting but can only withstand an output short to ground if, during the short, the output current is negative as often as positive during each 100 ms period. It is not short-circuit-proof under all conditions. Maximum continuous junction temperature should be kept below +150°C.

The case-to-ambient thermal resistance of the TO-3 package is θ_{CA} = 35°C/W. For the two output transistors, θ_{JC} is 95°C/W. With a 20 V_{P-P} output sinusoid, the effective θ_{JC} of these two transistors is 65°C/W. A heat sink is required above +75°C ambient (+85°C for sinusoidal output) if a 200Ω load is used. With a 100Ω load, a heat sink is required above +40°C ambient (+50°C for sinusoidal output).

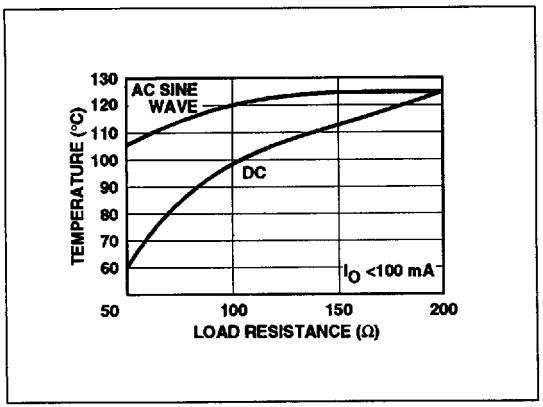

Figure 14. Maximum Allowable Case Temperature vs Load Resistance With Worst-Case Power Dissipation

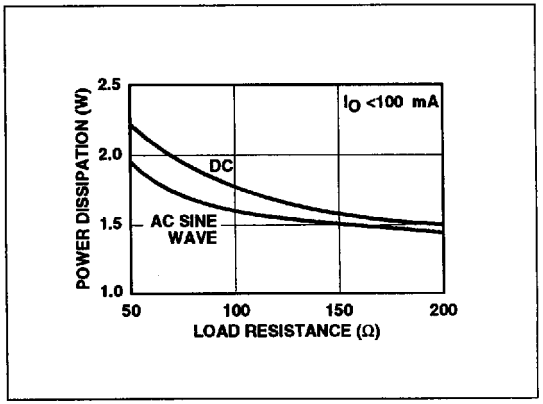

Figure 15. Worst-Case Power Dissipation vs Load Resistance

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